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AUTOMATIC INDUSTRIAL AIR POLLUTION MONITORING SYSTEM

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ABSTRACT

The level of pollution has increased with times by lot of factors like the increase in population, increased vehicle use, industrialization and urbanization which results in harmful effects on human wellbeing by directly affecting health of population exposed to it. In order to monitor In this project we are going to make an IOT Based Air Pollution Monitoring System in which we will monitor the Air Quality over a web server using internet and will trigger a alarm when the air quality goes down beyond a certain level, means when there are sufficient amount of harmful gases are present in the air like CO2, smoke, alcohol, benzene and NH3. It will show the air quality in PPM on the LCD and as well as on webpage so that we can monitor it very easily. In this IOT project, you can monitor the pollution level from anywhere using your computer or mobile.

Key Words: Internet of things, air pollution, sound pollution, sensors, monitoring system,aurduino

INTRODUCTION

The main objective of IOT Air & Sound Monitoring System is that the Air and sound pollution is a growing issue these days. It is necessary to monitor air quality and keep it under control for a better future and healthy living for all. Due to flexibility and low cost Internet of things (IoT) is getting popular day by day. With the urbanization and with the increase in the vehicles on road the atmospheric conditions have considerably affected. Harmful effects of pollution include mild allergic reactions such as irritation of the throat, eyes and nose as well as some serious problems like bronchitis, heart diseases, pneumonia, lung and aggravated asthma. Monitoring gives measurements of air pollutant and sound pollution concentrations, which can then be analyzed interpreted and presented. This information can then be applicable in many ways. Analysis of monitoring data allows us to assess how bad air pollution and sound pollution is from day to day.

EXISTING MODEL

The commercial meters available in the market are Fluke CO220 carbon monoxide meter for CO, Amprobe CO2 meter for CO2, ForbixSemicon LPG gas leakage sensor alarm for LPG leakage detection. The researchers in this field have proposed various air quality monitoring systems based on WSN, GSM and GIS. Now each technology has limited uses according to the intended function, as Zigbee is meant for users with Zigbee trans-receiver, Bluetooth. GIS based system is designed, implemented and tested to monitor the pinpoints of air pollution of any area. It consists of a microcontroller, gas sensors, mobile unit, a temporary memory buffer and a web server with internet connectivity which collects data from different locations along with coordinate's information at certain time of a day. The readings for particular location are averaged in a closed time and space. The Global Positioning System (GPS) module is attached to a system to provide accurate representation of pollution sources in an area. The recorded data is periodically transferred to a computer through a General Packet Radio Service (GPRS) connection and then the data will be displayed on the dedicated website with user acceptance.

ARDUINO

Arduino is an open-source electronics platform based on easy-to-use hardware and software. Arduino boards are able to read inputs - light on a sensor, a finger on a button, or a Twitter message - and turn it into an output - activating a motor, turning on an LED, publishing something online. All Arduino boards are completely open-source, empowering users to build them independently and eventually adapt them to their particular needs. The software, too, is open-source, and it is growing through the contributions of users worldwide.

AIR QUALITY PARAMETERS

The important parameters that are considered in the proposed framework include: • Carbon Dioxide (CO2) – CO2 is colorless, odorless gas and non-combustible gas. Moreover, it is considered under the category of asphyxiate gases that have capability of interfering the availability of oxygen for tissues. Carbon Dioxide is a gas essential to life in the planet, because it is one of the most important elements evolving photosynthesis process, which converts solar into chemical energy. The concentration of CO2 has increased due mainly to massive fossil fuels burning. This increase makes plants grow rapidly. The rapid growth of undesirable plants leads to the increase use of chemicals to eliminate them. • Sulphur Dioxide (SO2) - Sulphur Dioxide is a colorless gas, detectable by the distinct odour and taste. Like CO2, it is mainly due to fossil

fuels burning and to industrial processes. In high concentrations may cause respiratory problems, especially in sensitive groups, like asthmatics. It contributes to acid rains. • Nitrogen Dioxide (NO2) – Nitrogen Dioxide is a brownish gas, easily detectable for its odour, very corrosive and highly oxidant. It is produced as the result of fossil fuels burning. Usually NO thrown to the atmosphere is converted in NO2 by chemical processes.

AIR POLLUTION MONITORING EQUIPMENT

The different components of the equipment along with their intended purpose are discussed below: • Arduino Uno R3 microcontroller It is the most flexible hardware platform used based on ATmega328P which can be programmed according to the function where it is to be used. It has 6 analog inputs, 14 digital input/output pins (6 pins of these can be used as PWM outputs), a USB Connection, a 16 MHz quartz crystal, SPI, serial interface, a reset button, a power jack and an ICSP header as shown in Fig.3.The Arduino microcontroller is not only for technical audience but is intended for designers and artists as well because of its focus to usability based on its design which helps to achieve the intended goal the primary component of the framework. In addition, it is an open source microcontroller device with easily accessible software/hardware Platform and is compatible with many sensors available. Everything needed for its working is present on the board; we only require a USB cable to directly connect it to the computer or give power using battery source or AC to DC adapter to get started.

WORKING

We start with connecting the ESP8266 with the Arduino. ESP8266 runs on 3.3V and if you will give it 5V from the Arduino then it won't work properly and it may get damage. Connect the VCC and the CH_PD to the 3.3V pin of Arduino. The RX pin of ESP8266 works on 3.3V and it will not communicate with the Arduino when we will connect it directly to the Arduino. So, we will have to make a voltage divider for it which will convert the 5V into 3.3V. This can be done by connecting three resistors in series like we did in the circuit. Connect the TX pin of the ESP8266 to the pin 10 of the Arduino and the RX pin of the esp8266 to the pin 9 of Arduino through the resistors. ESP8266 Wi-Fi module gives your projects access to Wi-Fi or internet. It is a very cheap device and makes your projects very powerful. It can communicate with any microcontroller and it is the most leading devices in the IOT platform. Learn more about here. Then we will connect the MQ135 sensor with the Arduino. Connect the VCC and the ground pin of the sensor to the 5V and ground of the Arduino and the Analog pin of sensor to the A0 of the

Arduino. Connect a buzzer to the pin 8 of the Arduino which will start to beep when the condition becomes true. The MQ135 sensor can sense NH3, NOx, alcohol, Benzene, smoke, CO2 and some other gases, so it is perfect gas sensor for our Air Quality Monitoring Project. When we will connect it to Arduino then it will sense the gases, and we will get the Pollution level in PPM (parts per million). MQ135 gas sensor gives the output in form of voltage levels and we need to convert it into PPM. So for converting the output in PPM, here we have used a library for MQ135 sensor, it is explained in detail in "Code Explanation" section below. Sensor was giving us value of 90 when there was no gas near it and the safe level of air quality is 350 PPM and it should not exceed 1000 PPM. When it exceeds the limit of 1000 PPM, then it starts cause Headaches, sleepiness and stagnant, stale, stuffy air and if exceeds beyond 2000 PPM then it can cause increased heart rate and many other diseases. When the value will be less than 1000 PPM, then the LCD and webpage will display "Fresh Air". Whenever the value will increase 1000 PPM, then the buzzer will start beeping and the LCD and webpage will display "Poor Air, Open Windows". If it will increase 2000 then the buzzer will keep beeping and the LCD and webpage will display "Danger! Move to fresh Air".

CONCLUSION

The system to monitor the air of environment using Arduino microcontroller, IOT Technology is proposed to improve quality of air. With the use of IOT technology enhances the process of monitoring various aspects of environment such as air quality monitoring issue proposed in this paper. Here the using of MQ135 gas sensor gives the sense of different type of dangerous gas and arduino is the heart of this project which controls the entire process. Wi-Fi module connects the whole process to internet and LCD is used for the visual Output. The Automatic Air & Sound management system is a step forward to contribute a solution to the biggest threat. The air & sound monitoring system overcomes the problem of the highly-polluted areas which is a major issue. It supports the new technology and effectively supports the healthy life concept. This system has features for the people to monitor the amount of pollution on their mobile phones using the application.

BIBLOGRAPHY:

- The 8051 Micro controller and Embedded Systems
  - MuhammadAliMazidi
  - JaniceGillispieMazidi
- The8051MicrocontrollerArchitecture,Programming& Applications
  - KennethJ.Ayala
- Fundamentals of Micro processors and Micro computers
  - B. Ram
- Electronic Components
  - D.V.Prasad

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WASTE MANAGEMENT USING NODE MCU

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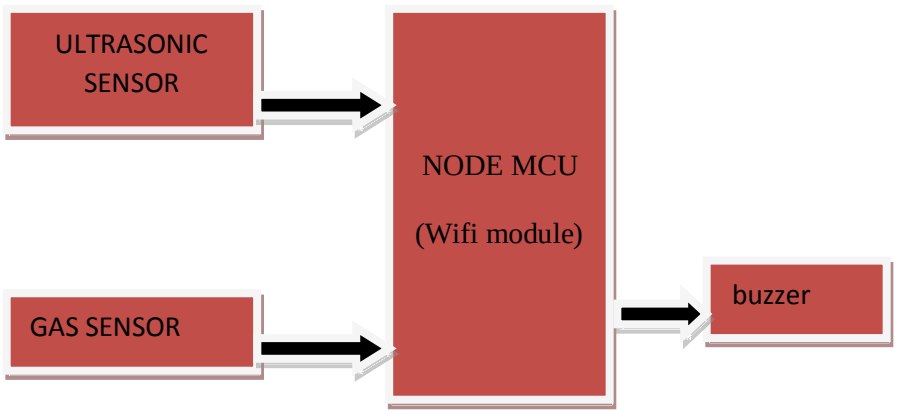
ABSTRACT

Appropriate technology should be used for waste management. Technology should be friendly to environment , affordable to user and it should be accepted by society. Evolution of IoT paved a path of managing and recycling the waste efficiently. The paper deals with waste management system with sensors and cloud. The sensors are used to identify the levels of waste in the bin. If the bin is full, notifications are sent to the truck driver by cloud and Wi-Fi. The truck driver collects the waste and transfer it to the main storage, where the decomposition of the waste is carried out using gas sensor. The location of the bin is identified. All the details are displayed remotely using the cloud. The main idea of the paper is to manage the waste and recycle the waste and use it for fertilizer.

BLOCK DIAGRAM:



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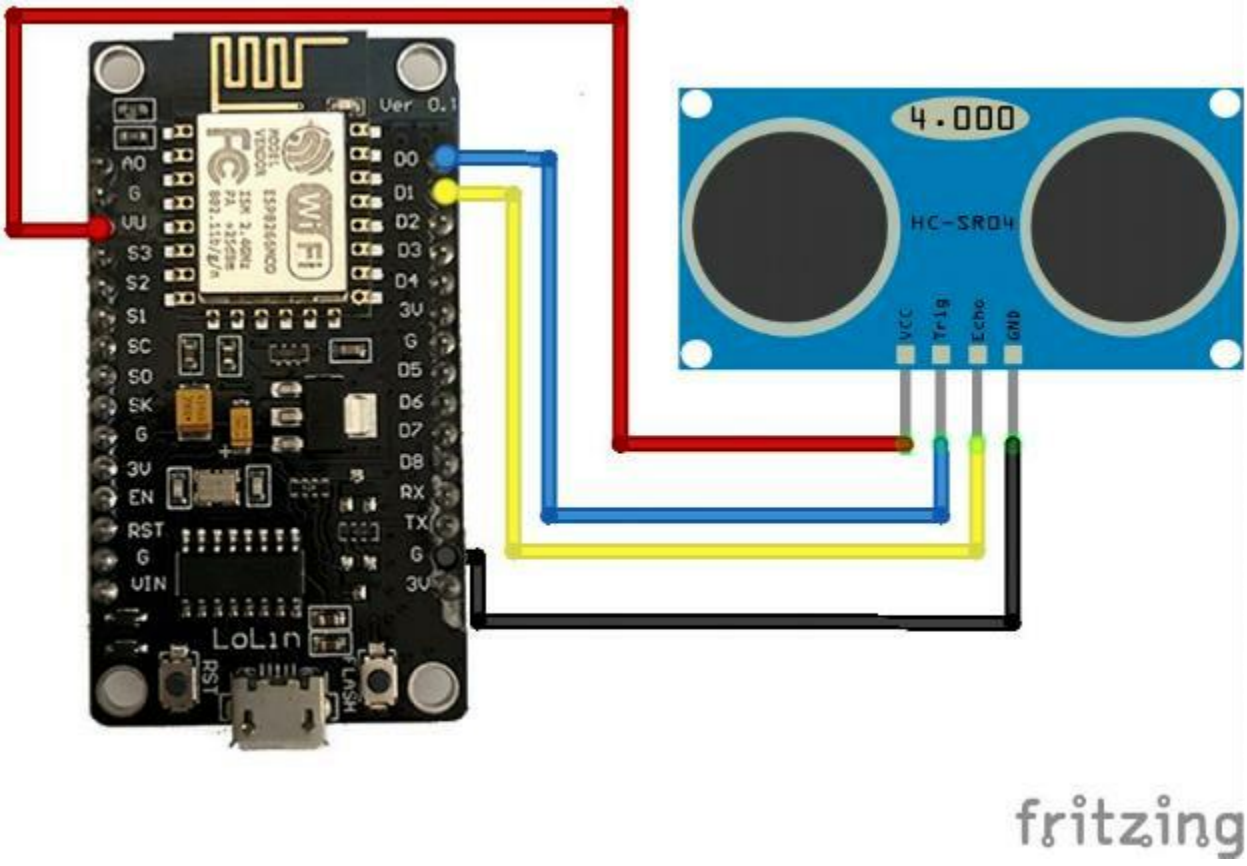
HARDWARE REQUIREMENTS:

- Node MCU
- Ultrasonic sensor
- Gas sensor
- Buzzer
-

SOFTWARE REQUIREMENT:

- Arduino IDE
- Buzzer
- Embedded C
- Blynk android app

CIRCUIT:



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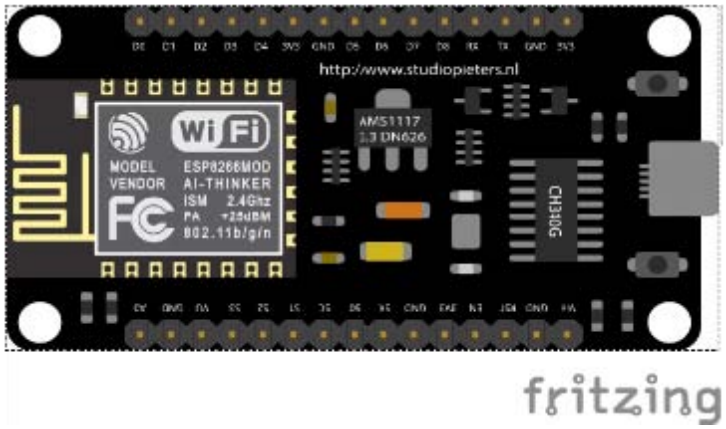
NODEMCU



The best way to develop quickly an IoT application with less Integrated circuits to add is to choose this circuit "NodeMCU". Today,we will give a detailed Introduction on NodeMCU V3. It is an open-source firmware and development kit that plays a vital role in designing a proper IoT product using a few script lines.
The module is mainly based on ESP8266 that is a low-cost Wi-Fi microchip incorporating both a full TCP/IP stack and microcontroller capability. It is introduced by manufacturer Espressif Systems. The ESP8266 NodeMcu is a complex device, which combines some features of the ordinary Arduino board with the possibility of connecting to the internet.

Arduino Modules and Microcontrollers have always been a great choice to incorporate automation into the relevant project. But these modules come with a little drawback as they don't feature a built-in WiFi capability, subsequently, we need to add external WiFi protocol into these devices to make them compatible with the internet channel.

This is the famous NodeMCU which is based on ESP8266 WiFi SoC. This is version 3 and it is based on ESP-12E (An ESP8266 based WiFi module). NodeMCU is also an open-source firmware and development kit that helps you to prototype your IOT product within a few LUA script lines, and of course you can always program it with Arduino IDE.

In this article, We will try present useful details related to this WiFi Development Kit, its main features, pinout and everything we need to know about this module and the application domain.

Humidity and Temperature detection
The bin temperature and humidity should be monitored because it may cause the waste in the bin to decompose and cause pungent smell from the bin which may cause many diseases. So that we use a DHT11 sensor to analyze the temperature and humidity of the bin. This can be visualized using cloud.

CONCLUSION

We presented an intelligent waste collection system. The system is based on IoT sensing prototype. It is responsible for measuring the waste level in the waste bins and later send this data (through Internet) to a cloud for storage and processing. This data helps to compute the amount of waste and how it is decomposed. The waste collected can also be used as a fertilizer in future.

REFERENCES

1. B. Chowdhury and M. U. Chowdhury, "RFID-based realtime smart waste management system," in Proceedings of the Telecommunication Networks and Applications Conference, pp.175–180, December 2007.

2. Delicato F. C., Pires P. F., Batista T., Cavalcante E., Costa B., Barros T., "Towards an IoT eco-system", In the Proceedings of the 1st ACM International Workshop on Software Engineering for Systems-of-Systems, SESoS'13, pp. 25-28, Montpellier, France, July, 2013.

3. Guerrero L. A., Maas G., Hogland W., "Solid waste management challenges for cities in develop-ing countries", Journal of Waste Management, vol. 33 (1), pp. 220-232, January, 2013.

4. L.Mashayekhy, et al., "Incentive-compatible online mechanism for resource management",Proceedings of 7th International Conference on Cloud Computing, IEEE, Alaska, USA, 2014, pp. 56-61.

5. Marshall R. E., Farahbakhsh K., "Systems approaches to integrated solid waste management in developing countries", Journal of Waste Management, vol. 33 (4), pp. 988-1003, April, 2013.

6. Palaghat Yaswanth Sai. proposed"IOT Smart Garbage Monitoring System in Cities-An Effective Way to Promote Smart City",

7. Prof. Dr. Sandeep M. Chaware, Shriram Dighe, Akshay Joshi, Namrata Bajare, Rohini Korke proposed "Smart Garbage Monitoring System using Internet of Things (IOT) ",

8. Qiang Duan, et al., "A survey on service-oriented network virtualization towards convergence of networking and IoT", Transactions on Network and Service Management, IEEE, Vol. 9, No. 4, 2012, pp. 373-392.

9. Rajput "Scenario of Solid WasteManagement," IEEE Journal on Emergingand Selected Topics in Circuits and Systems, vol. 3, no. 1, pp. 45–54, 2009.

CMS for pandemic situation using IIoT and CAN

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ABSTRACT

Controller Area Network (CAN) is an effective choice for the automotive industries due to its simplicity, low cost nature, and in addition to that it provide connectivity with multiple nodes with single wiring pair. This project aims in describing an ARM 7 LPC 2148 based Industrial monitoring system with Controller Area Network (CAN) bus. Objective of this project is to construct a hardware proposal for communication between nodes with CAN bus. A Node to Node communication link has been established which are connected via CAN bus so as to observe and control the sensor values, by transferring the sensor values on the CAN bus and send the control signals to actuators and indicators. The proposed system also provide the measurement of contactless temperature of the person to alert the entry of person who has high body temperature. The CAN communication module can transmit or receive data following CAN Protocol. With the help of the software used, the CAN-BUS communication would be clear to the nodes of the ARM 7 Controllers in the system. The software part is done in KEIL µvision-4 using Embedded.

Keywords: ARM7, CAN, IIOT, Sensors, Actuators

INTRODUCTION

Nowadays industrial automation systems have become popular in many of the industries and play a crucial role in controlling several process-related operations. Due to the implementation of a wide variety of industrial networks with their geographical distribution over factory or industry, the floor data transferring and controlling capability has become more sophisticated and easy ranging from low-level to high-level control. These industrial networks are routed through various field buses that use various communication standards like CAN protocol, Profibus, Modbus, Device net, etc. So let us look on how CAN communication works for automating the industries and other automation based systems.

Introduction to Industrial Automation and Control

The below figure shows the architecture of industrial automation and control wherein three levels of control is performed to automate the whole system. These three levels are control and automation, process control, and higher-order control. The Control and Automation level consists of various field devices like sensors and actuators to monitor and control the process variables.

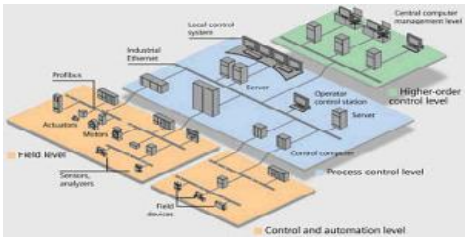


Fig1. Industrial Automation Architecture

Process Control Level is a central controller responsible for controlling and maintaining several controlling devices like Programmable Logic Controllers (PLCs), and also the User Graphical Interfaces like SCADA and Human Machine Interface (HMI) are also included in this level. The Higher Order Control Level is an enterprise level that manages all business related operations.

By closely observing the above diagram and its each and every level and also in-between levels, the communication buses such as Profibus and industrial Ethernet are seen as connected to exchange the information. Therefore, the communication bus is the major component in industrial automation for reliable transfer of data among the controllers, computers and also from the field devices.

Control Area Network or CAN Protocol

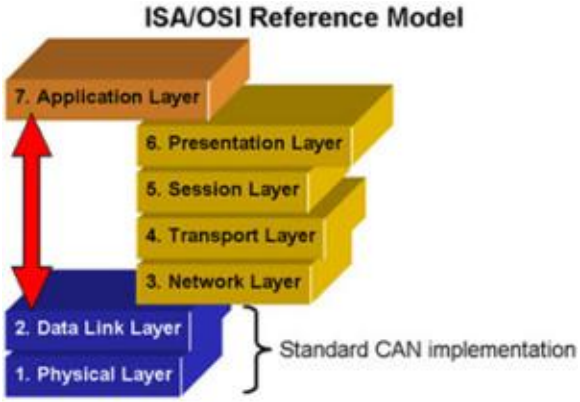


Fig2. Open Systems Interconnection (OSI) model

Data communication is the transfer of data from one point to another. To support industrial communication, International Organization for Standardization has developed Open Systems Interconnection (OSI) model for providing data transfer between various nodes. This OSI protocol and framework depends on the manufacturer. The CAN protocol uses lower two layers i.e., physical and data link layers out of the seven layers of the OSI model.

A Controller Area Network, or CAN protocol is a multi-master serial communication bus, and it is a network of independent controllers. The current version of CAN has been in usage since 1990, and it was developed by Bosch and Intel. It broadcasts messages to the nodes presented in a network by offering a transmission speed ranging up to 1 Mbps. For an effective transmission, it follows reliable error-detection methods – and, for arbitration on message priority and collision detection, it uses carrier sense multiple access protocol. Due to these reliable data transfer characteristics, this protocol has been in use in buses, cars and other automobile systems, factory and industrial automation, mining applications, etc

I. LITERATURE SURVEY

Industrial automation using CAN protocol [3][4] describe project is implemented to control the industrial loads that are run by DC motor based on the temperature variations of the process. Various process control systems are depends on the temperature. So this project achieves this with the use of CAN protocol which is highly efficient and reliable low-cost communication. Two microcontrollers are used in this project, one for acquiring temperature data and the other for controlling the DC motor. CAN Controller MCP2515[3][4] and CAN transceiver MCP2551 are connected to both microcontrollers to implement CAN communication for exchanging the data but disadvantage practically it is limited to 110 nodes due to the hardware transceivers. It supports cabling up to 250 meters.

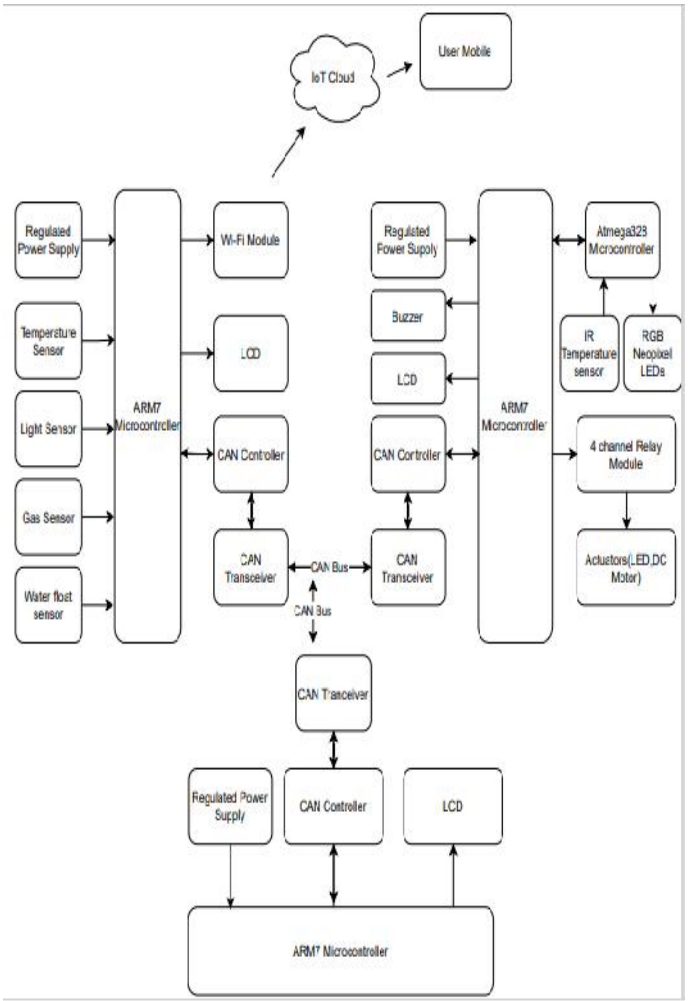
Industrial automation using ZigBee [2] describe the transmitter section, the Zigbee module is configured in such a way that it receives the data collected from the microcontroller and sends it to the remote receiver. In this system, the microcontroller is programmed to collect the data from an analog to digital converter that continuously monitors temperature, voltage and current parameters. At the receiver side, the Zigbee [2] module receives all the sent data from a Zigbee transmitter within the range of communication. This data is further transferred to the microcontroller using an embedded circuitry wherein the microcontroller program compares all these data parameters with predefined set limits. If any parameter exceeds its limit, then the microcontroller sends command signals to a relay driver IC, which is responsible to operate different loads such as motors, relays, circuit breakers, etc. All these parameters' information is also displayed on LCD display as a Human machine interface. In this way, industrial parameters can be easily monitored and controlled through the short range low cost and low powered Zigbee communication technology. It supports two ways communication between transmitting devices and controllers at 10-100 meters distance.

When it comes to temperature sensing, there are several variants of Arduino-based solutions. In [14][15], Arduino was used for real-time temperature visualization using MATLAB. However, the used sensor does not allow contactless temperature sensing. Moreover, in [21], a similar system incorporating the usage of smartphones for remote temperature monitoring using Arduino Uno was presented.

II. PROPOSED SYSTEM

The block diagram of proposed system is shown in Fig.3 one slave modules and one master module along with one special slave are present.

3.2BLOCK DIAGRAM



3.2 BLOCK DIAGRAM EXPLANATION:

(i) As shown in the fig3. The node1 consists of arm7 interfaced with temperature sensor, light intensity sensor, gas sensor and water level sensor along with LCD, wifi module and CAN Module. Here ARM7

continuously read the sensor data and display on the lcd and send to the CAN module by converting the sensor data into CAN message format. The arm microcontroller here also send the sensor information to Wi-Fi module which will update into thingspeak cloud.

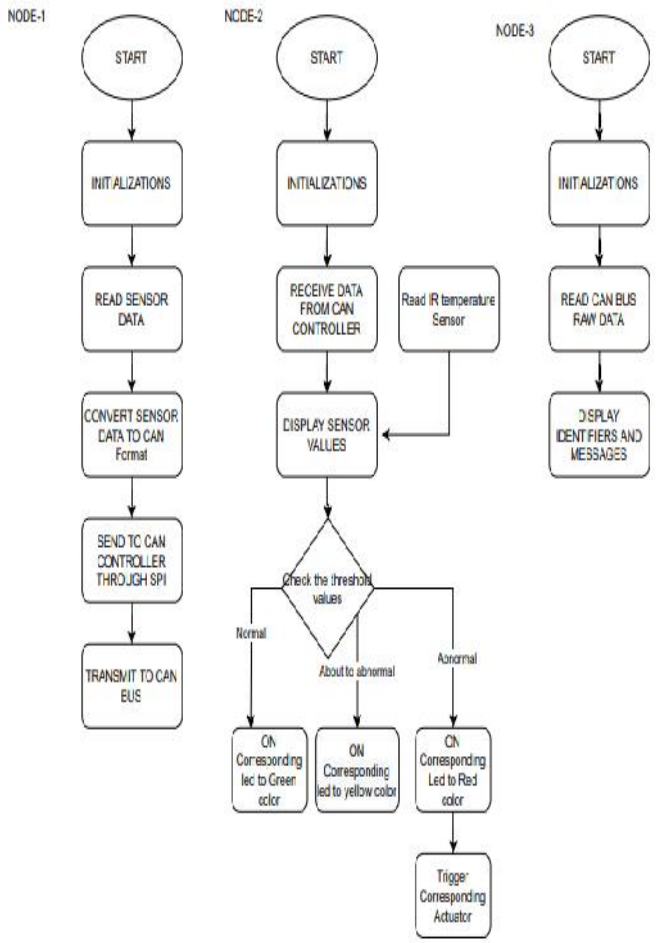
(ii). The second node of our proposed system consists of ARM7 microcontroller interfaced with contactless ytemperature sensor, CAN Module, RGB led's , Relay actuators along with LCD and Buzzer. Here the ARM processor receive the sensor information from CAN Module and read the contactless temperature sensor information and display the total information on the LCD. Here the microcontroller also analyze the sensor information based on predefined threshold levels and switching the buzzer alerts and corresponding indicator along with Actuator to control the particular parameter.

(iii). The third node of the proposed system consists of ARM7 microcontroller interfaced with CAN module and LCD. Here the ARM7 microcontroller read the raw data on CAN Bus and display on the LCD which will helps us to analyze the can protocol.

3.3 WORKING:

Always master only initiates the communication. Here the node 1 measures temperature, GAS, light intensity and water level value senses the those values to the monitor module via CAN protocol after converting values into digital values via Analog to Digital converter. Similarly the slave 2 is used to analyze the data over can bus. The master module and slave module both are displays all the sensor values on the LCD. If any sensor value crosses the threshold value, then the corresponding actuator and indicator led is automatically turned ON, and simultaneously the sensor information will be sent to a higher authority or supervisor regarding the abnormal situation via IoT (Internet of Things). If the temperature value is higher than the threshold value, the relay is turned to ON in order to cool the temperature. Similarly if smoke/gas level is higher than the threshold value, the buzzer is turned ON to indicate the abnormal condition.

3.4 FLOWCHART:



III. HARDWARE TOOLS USED

(a) ARM7(LPC2148) Microcontroller

(b) CAN MODULE (MCP2515 & MCP2551)

(c) 16x2 LCD

(d) LM35 Temperature sensor

(e) MQ2 Gas sensor

(f) LDR Sensor

(g) Float Sensor

(h) 4-Channel 5V relay Module

(i) Neopixel LEDs

(j) DC Motor

(k) Infrared Temperature sensor

(l) 5v and 3.3v regulated power supply

IV. SOFTWARE TOOLS USED

(a) Keil uVison4 IDE

(b) Flash Mazic

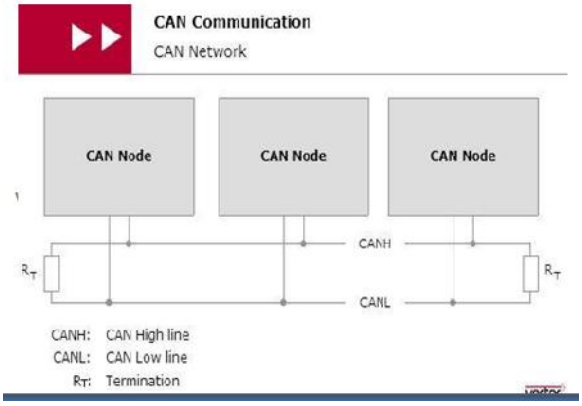
V. CAN PROTOCOL

(a). CAN Communication

CAN Network

A CAN network consists of a number of **CAN nodes** which are linked via a physical transmission medium (**CAN bus**) In practice, the CAN network is usually based on a**line topology** with a linear bus to which a number of electronic control units are each connected via a CAN interface. The passive star topology may be used as an alternative.

The maximum data rate is 1 Mbit/s. A maximum network extension of about 40

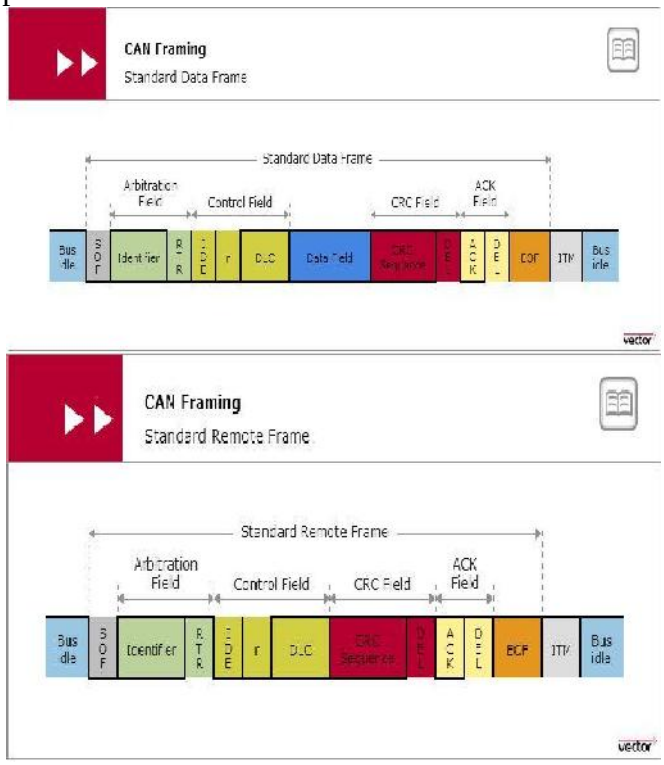


meters is allowed. At the ends of the CAN network, bus termination Resistors contribute to preventing transient phenomena (reflections). ISO 11898 specifies the maximum number of CAN nodes as 32.

CAN Framing

Frame Types

For transmitting user data, ISO 11898-1 prescribes the so-called data frame.



The error frame is available to indicate errors detected during communication. An ongoing erroneous data transmission is terminated and an error frame is issued. The layout of an error frame differs significantly from the structure of the terminated erroneous data or remote frame. It consists of just two parts: The error flag and the error delimiter.

VI. RESULT ANALYSYS

The proposed system was fully developed and tested to demonstrate its feasibility and effectiveness. The screenshots of the **CMS FOR PANDEMIC SITUATION USINGIIOT AND CAN** has been presented in Figures bellow.

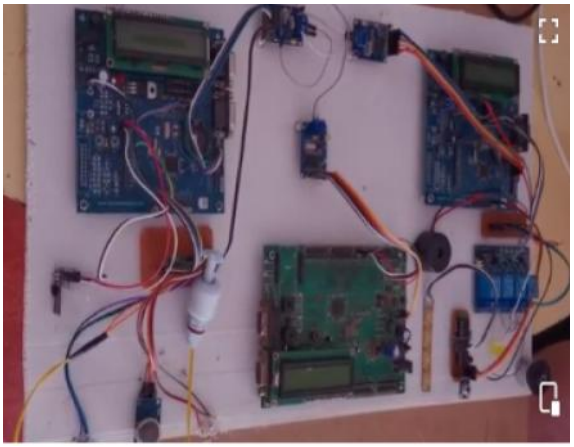


Fig. proposedsystem

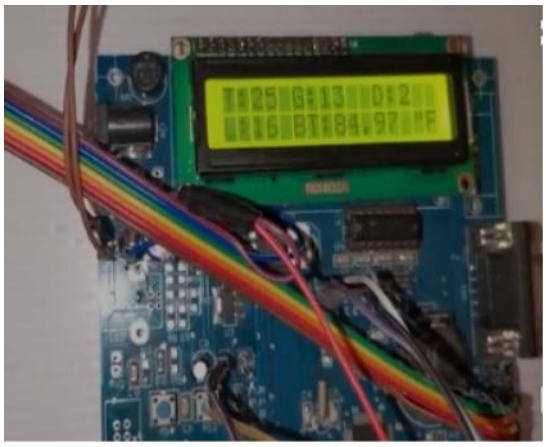


Fig. Displaying Sensor data

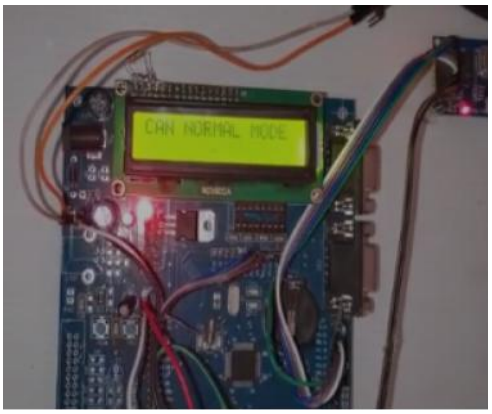


Fig. CAN Checking

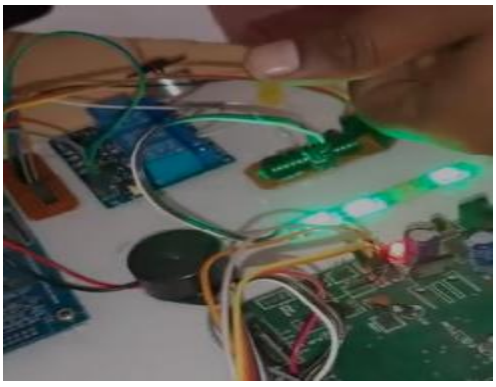


Fig. Indicators and Actuator Status

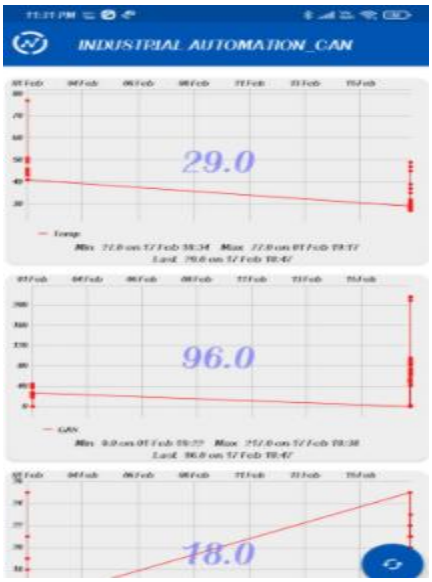


Fig. Screenshot of thingspeak cloud monitoring

VII. CONCLUSION

In this work we can conclude that by monitoring and controlling the industrial parameters like temperature, water level or fuel level, Gas and light with help of single node and internet server or mobile application. The system also designed to follow the covid19 rule over body temperature. Our objective is to eliminate the concept of huge control room required for monitoring and controlling above parameters, this can monitor from anywhere through the internet. This system also provides indication along with automatic control over the parameters increases over safe value, so the harmful situation may overcome through this project.

REFFERENCES:

[1] Andrea Zanella, Lorenzo Vangelista, "Internet of Things for Smart Cities" IEEE Internet of Things Journal, vol. 1, no. 1, February 2014.

[2] Minal Nikose, Pratibha Mishra, Avinash Agrawal, " A Review on Industrial Automation by Zigbee Based Wireless Remote Controller", International Journal of Scientific & Technology Research volume 3, issue 4, April 2014.

[3] P.Ram Babu, C.Madhusudan, "Industrial Automation and Control System Using Can Protocol". International Journal & Magazine of Engineering, Technology, Management and Research, Volume No: 2 (2015), Issue No: 12 (December).

[4] B.Meena Kumari1, M. Satya Sailaja, "Industrial Automation and Process Control System Using Can Bus", International Journal of Science and Research (IJSR) (2014).

[5] Ubaid saudagar, "Implementation of can protocol for industrial automation", IJSETR, international conference, INDIA, October-2014, Volume.03, IssueNo.31.

[6] Yeshwant Deodhe, Swapnil Jain, Ravindra Gimonkar. "Implementation of sensor network using efficient can interface" Volume 1, Issue 1, February 2014, IJCAT

[7] B. Meena Kumari, M. Satya Sailaja, " Industrial Automation and Process Control System Using Can Bus", IJSR, Volume 4 Issue 12, December 2015.

[8] Bhagyashree Dattatray Daware, Prof. Hatkar A, "IOT Based Industrial Monitoring and Fault Detection Using Android", IJIRCCE Vol. 5, Issue 6, June 2017.

[9] Dr. S.W Mohod, Rohit S Deshmukh," Internet of Things for Industrial Monitoring and Control Applications" IJIRCCE ,Volume 7, Issue 2, February-2016

[10] Sanket N. Gore1, Apeksha Sakhare2 "Design and automation of industrial machine using esp8266 module" IJRET, Volume: 06 Issue: 01 Jan-2017

[11] CH.Mounika K.S.Roy, Mahaboob Ali "Motor Speed Control Based On

Temperature Using Can Protocol", IJETT Volume4Issue4 April 2013

[12]MCP 2551 High speed CAN Transceiver Datasheet.

[13] MCP 2515 Stand-Alone CAN Controller with SP Interface datasheet [10] ATmega328/P datasheet

[14] R. Biswas, A. Roy, “Real Time Temperature Graph using MATLAB and Arduino”, International Journal of Engineering Research & Technology (IJERT) vol. 9 issue 5, pp. 624-625, 2020. https://doi.org/10.17577/IJERTV9IS050482

[15] Thermal Sensors for Contactless Temperature Measurements, Occupancy Detection, and Automatic Operation of Appliances during the COVID-19 Pandemic: A Review

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A REVIEW ON LOW POWER 1-BIT FULL ADDER USING FULL-SWING GATE DIFFUSION INPUT TECHNIQUE

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ABSTARCT

This project presents a design which provides full swing output for logic 1 and logic 0 for 1-bit full adder cell and reduces power consumption, delay, and area. In this design full adder consists of GDI input cell. The performance of the proposed design compared with the different logic style for full adders through DSCH simulation based on PTL design technology models with a supply voltage of 1v and frequency 125MHz with only 10 transistors. The simulation results showed that the proposed full adder design dissipates low power, while improving delay and area among all the design taken for comparison.

INTRODUCTION

Lately, the rapid advance in multimedia and digital communication systems, real time signal processing like audio signal processing, image and video processing are heavily needed. Many applications such as Processors and Digital Signal Processing operations such as Filtering, Convolutional transformation, require some form of addition such as multiplication, multiply and accumulate operation (MAC) and subtraction. The 1-bit full adder cell is the main block in all these modules [1]. Because of the need in portable devices such as laptop and cell phones for low power consumption. The power consumption, small area and high speed are the crucial factors to be considered in VLSI design with high performance [2]. There were many techniques to design in VLSI circuit and minimize the power and area, but their best gate diffusion input technique The aim of this work is to design 1-bit full adder circuit using full-swing GDI to reduce power consumption, delay and area, in addition to achieve full-swing output.

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application specific DSP architectures and microprocessors. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder is

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part of the critical path that determines the overall performance of the system. That is why enhancing the performance of the 1-bit full-adder cell (the building block of the binary adder) is a significant goal. Recently, building low-power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology doesn't advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption. So building low-power, high-performance adder cells is of great interest. The power consumption breakdown in a modern day high-performance microprocessor. The data path consumes roughly 30% of the total power of the system. Adders are an extensively used component in data paths and, therefore, careful design and analysis is required for these units to obtain optimum performance. On the other hand, as discussed in [4], we can see from the that clock signals consumes 45% of the total power, which is very high in fact. As power dissipation has become one of the most important constraints in the design flow of modern processors, therefore, under this common scenario, it has become extremely important to consider the power consumption of any proposed module when there are non-transitioning input data or there is no clock signal activity.

LITERATURE SURVEY

In 2002 [3] A. Morgenshtein, A. Fish and A. Wagner proposed Gate Diffusion Input Technique (GDI) for low power and small silicon area of VLSI digital design as an alternative to CMOS logic design. Presented in figure 2.1 (a) Primitive Proposed GDI cell

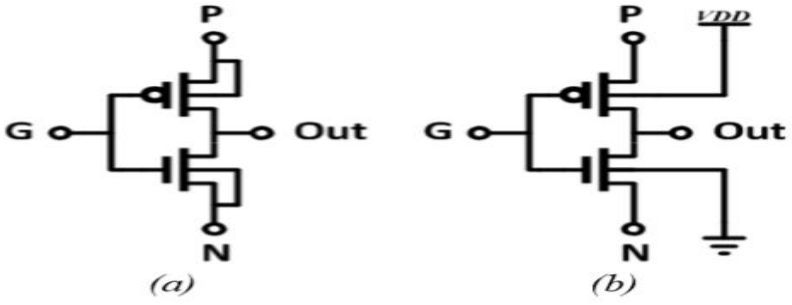

Fig.2.1 GDI cell; (a) Primitive Proposed GDI Cell, (b) MOD-GDI

The most common problem with PTL technique is its low voltage swing. An extra buffer circuitry may be used additionally to eliminate the problem of low swing and improve drivability. The problem of low swing can be understood with the help of a random function.

Actually, this technique proposed for fabrication in silicon on insulator (SOI) and twin-well

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CMOS processes. Also, it provides an effective way for the design of fast, low power design using less number of transistors as compared to CMOS, PTL and TG techniques. This allows the design of many complex functions using only 2 transistors as listed in table 2.1.

The below table 2.1 the various function of the GDI input technique where the output of the each function at different conditions are described.

Table 2.1 DESIGN OF COMPLEX FUNCTIONS

N	P	G	OUT	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{\ }+B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
0	1	A	$\overline{\ }$	NOT

This paper proposes a 3T XOR gate design implemented using pMOS transistors only. The design has been compared with existing design and significant improvement in power consumption has been obtained. All pre layout simulations are performed on 45nm standard model on Tanner EDA tool version 13.0.

Rajkumar Sarma and Veerati Raju proposed Adder cells using Gate Diffusion Technique (GDI) & PTL-GDI technique are described in this paper. GDI technique allows reducing power consumption, propagation delay and low PDP (power delay product) whereas Pass Transistor Logic (PTL) reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Performance comparison with various Hybrid Adder is been presented. In this paper, we propose two new designs based on GDI & PTL techniques, which is found to be much more power efficient in comparison with existing design technique. Only 10 transistors are used to implement the SUM & CARRY function for both the designs.

The SUM and CARRY cell are implemented in a cascaded way i.e. firstly the XOR cell is implemented and then using XOR as input SUM as well as CARRY cell is implemented. For Proposed GDI adder the SUM as well as CARRY cell is designed using GDI technique. On the other hand in Proposed PTL-GDI adder the SUM cell is constructed using PTL technique and the CARRY cell is designed using GDI technique. The advantages of both the designs are discussed. The significance of these designs is substantiated by the simulation results obtained from Cadence Virtuoso 180nm environment.

This logic style was suffering from some limitations such as reduced output voltage swing due

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to the threshold drops, this means that the output either high or low voltage is deviated from VDD or GND by threshold voltage drop (Vth), as that threshold drop causes performance degradation and increases short circuit power.

To solve this problem Morgenshtein, Shwartz and Fish [4] proposed modified gate diffusion input logic style (MODGDI) the cell is similar to basic cell of GDI, but have important difference in MOD-GDI, the substrate terminals of NMOS and PMOS connected to GND and VDD, respectively, as shown in figure 2.1(b). This logic is compatible for implementation in a standard CMOS process, and achieves improvement in output, power and power delay product compared to the basic GDI logic. W, while the threshold drop problem, not fully resolved, but the output still has degraded still degrades the output.

In [5] Morgenshtin proposed a new approach to improve the output swing and overcome the threshold drop problem known as Full Swing (FS) GDI technique and utilizes only swing restoration transistor (SR) to ensure the full swing operation for F1 and F2 function. Either F1 or F2 gates or a combination of both can be used to realize any logical function. Although this technique uses more transistors than standard GDI but compared to CMOS logic style it uses a fewer number of transistors and achieves full swing output, low power, less delay and small area of the circuit.

SIMULATION RESULTS AND COMPARISON

The proposed 1-bit Full Adder circuit was designed using an PTL of GDI input cell. The simulations were done using the DSCH 3.5 software with low power supply of 1V and frequency 125MHz, the size of PMOS is twice the NMOS transistor size Wp/L=240/60, Wn/L=120/60 (PMOS and NMOS respectively) to achieve the best power and delay performance.

Fig.8.1 shows the waveform of the proposed Full Adder, The results of the proposed design compared with the designs in References [4] , [5] and [6] are shown in Table 7.1. Compared to the previous designs, the proposed design for 1-bit full adder consumes low power as that needed to least number of transistors to building circuits and present full swing output and less delay.

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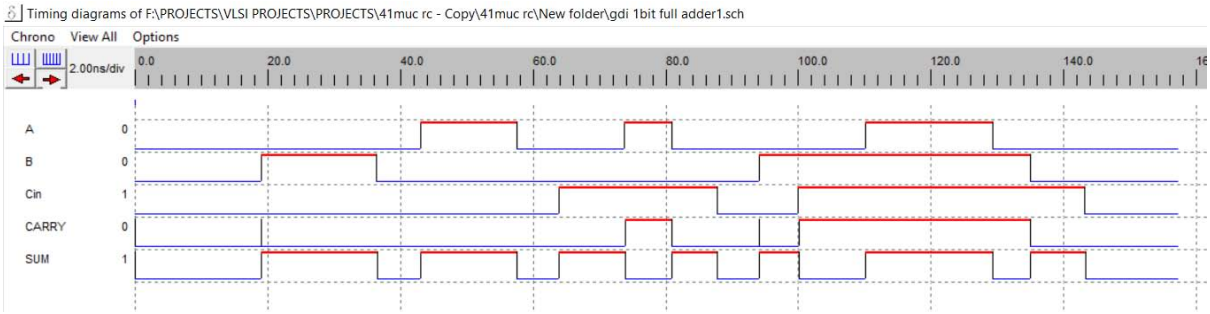
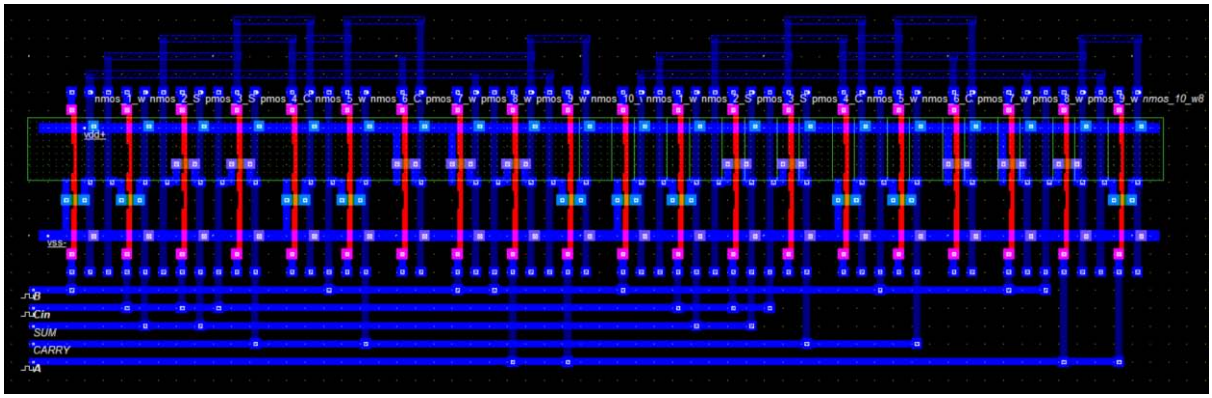
COMPARISION OF SIMULATION RESULTS.

Design	No.of Transistors	Power (nW)	Delay (ps)	Supply Voltage
Shoba.2016[9] Design1	18	927.9 nW	37.86	1.1V
D.shindi [10]	10	8100 nW	6.47	-
Shoba 2014 [11]	21	9000 nW	18	1.2
Existing design	16	693.5 nW	2.5	1V
Proposed design	10	693.5 nW	2.5	1V

The proposed 1-bit Full adder GDI cell system consists of only 10 transistors where the existing system consists of 16 transistors. This make the design of 1-bit GDI input full adder has more area efficient at same power efficient than the existing system.



The waveform of the proposed Full Adder



The layout diagram of the proposed system using Microwind2

The delay in 1 bit full adder using GDI input technique is 40.04 ps where 130.6 ps in CMOS design style.

CONCLUSION

This research work presents a 1-bit Full Adder designed using the Full-Swing GDI technique of pass transistor logic and simulated using the DSCH and Verilog file is compiled using Micro wind. Simulation results showed design in terms of power consumption and transistor count, while maintaining Full-Swing Operation. The proposed 1 bit GDI cell full adder design consists of only 10 transistors and operates under very low supply voltage with less area.

REFERENCES

[1] Tripti Sharma, K.G.Sharma and B.P.Singh,"High Performance Full Adder Cell: A Comparative Analysis",2010 IEEE Students' Technology Symposium 3-4 April 2010,IIT Kharagpur, 2010.

[2] Rajkumar Sarma1 and Veerati Raju," Design and Performance Analysis of Hybrid Adders For High Speed Arithmetic Circuit", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.

[3] A. Morgenshtein, A. Fish, and I. Wagner, “Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems IEEE Trans. VLSI Syst., vol. 10, no. 5, pp. 566–581, 2002.

[4] A. Morgenshtein, I. Shwartz, and A. Fish, “Gate Diffusion Input (GDI) logic in standard CMOS Nanoscale process,” 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel, 2010.

[5] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Fullswing gate diffusion input logic—Case-study of low-power CLA adder design," Integration, the VLSI Journal, vol. 47, no. 1, pp. 62–70, Jan. 2014.

[6] Korraravikumar, AL Reddy, M.Sadanandam, Santhoshkumar.A and M.Raju," Design of 2T XOR Gate Based Full Adder Using GDI Technique", International Conference on Innovative Mechanisms for Industry Applications (ICIMIA 2017),2017.

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A REVIEW ON PRACTICAL IMPLEMENTATION OF AREA EFFICIENT, LOW POWER AMBA-APB BRIDGE FOR SOC

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ABSTRACT

In this paper, we present the design of Advanced Peripheral Bus (APB) controller (or APB Bridge). UART as an APB slave has been used in the design. Linear Feedback shift register (LFSR) module has been included in the UART design for data security. We have also compared APB Bridge design compatible with AMBA Specification (Rev 2.0) and APB Bridge design compatible with AMBA 3 APB Specification (v1.0) for power and area constraints have been done. Design of APB Bride with AMBA3 APB save 6% power and 10% area over the one designed with AMBA2 APB.

Keywords

System-on-Chip (SOC); Advanced Microcontroller Bus Architecture (AMBA); Advanced Peripheral Bus (AMBA APB); Intellectual Property (IP); Universal Synchronous Transmitter Receiver (UART).

INTRODUCTION

Advanced Microcontroller Bus Architecture (AMBA) specification defines an on chip communication standard for designing high performance embedded microcontroller processors or systems. Advanced Microcontroller Bus Architecture specifications provide technology independent solution for communication between master and its slaves. AMBA specification is classified into Advanced High Performance Bus (AHB), Advanced System Bus (ASB) and Advanced Peripheral Bus (APB) with recent addition of Advanced Extensible Bus (AXI). Each bus type has its different application and advantages. AHB, ASB and AXI are high performance and high clock frequency system modules; APB is used for low power peripherals. APB can provide an effective media of communication/synchronization between the high performance/high bandwidth buses with low power peripherals (APB Bridge). APB Bridge provides zero power interfaces in static mode. APB can be used in along with any of the other buses (master) and APB acting as a slave. AMBA APB is optimized in such a way that the peripheral which is interfaced will consume minimum power and will also reduce the complexity of the interfacing circuit. The AHB or ASB signals received are converted

to APB signals by the APB Bridge and are fed to the APB slave (UART) to trigger particular application. A comprehensive work has been done with regards to designing of AMBA 2 APB Bridge for various peripherals (UART, TIMER) and the work done in is limited to hardware implementation of APB Bridge on FPGA. Less research has been done on designing an AMBA 3 APB Bridge along with secure communication. With new AMBA specifications coming up with time, in this work we propose architecture for AHB-APB Bridge with AMBA3 APB.

APB comes under AMBA 3 protocol family. AMBA specifications standards are used for designing highlevel embedded microcontrollers and it provides independence in technology and to encourage the modular system design. An AMBA protocol strongly encourages to reuse peripheral devices to minimize the silicon infrastructure. There are lots of protocols that comes under AMBA protocol ex:(CHI,ACE,AXI,AHB,ASB,APB). The APB- Advanced peripheral bus protocol is actually a part of the Advanced Bus Architecture protocol family (AMBA). It is defined as a less priced interface because of its optimization for less consumption of power and less complexity of interface. APB (advanced peripheral bus) is non-pipelined, used for connection with low bandwidth peripheral which does not require the AXI (high performance) protocol. To simply the integration of APB peripherals into a design flow it relates a signal transition to the rising edge of the clock. Each transfer takes at least two Cycles (setup cycle and access cycle). It can be used for accessing the programmable control registers of the peripheral devices.The APB can be interfaced with AMBA AHB (Advanced high performance bus), AMBA AHBLite (Advanced high performance bus lite), AMBA AXI (Advanced extensible interface), AMBA AXI4- lite (Advanced extensible interface lite) .

LITERATURE SURVEY

Architecture (AMBA) specification defines an on chip communications standard for designing high-performance embedded microcontrollers. AMBA has 4 versions as follows 1. VER1.0 (ASB & APB) 2. VER 2.0 (AHB) 3. VER 3.0 (AXI, ATB) 4. VER 4.0 (AXI 4,AXI LITE,AXI STREAM (AXI)) AMBA 4.0 specification buses/interfaces 1. Advanced eXtensible Interface (AXI) 2. Advanced High-performance Bus (AHB) 3. Advanced System Bus (ASB) 4. Advanced Peripheral Bus (APB) 5. Advanced Trace Bus (ATB) In this project these are to be used Advanced eXtensible Interface (AXI4-Lite) & Advanced Peripheral Bus (APB) because these are high bandwidth data transfer between high performance devices like processor, DMA, RAM etc..,. and Peripheral devices.

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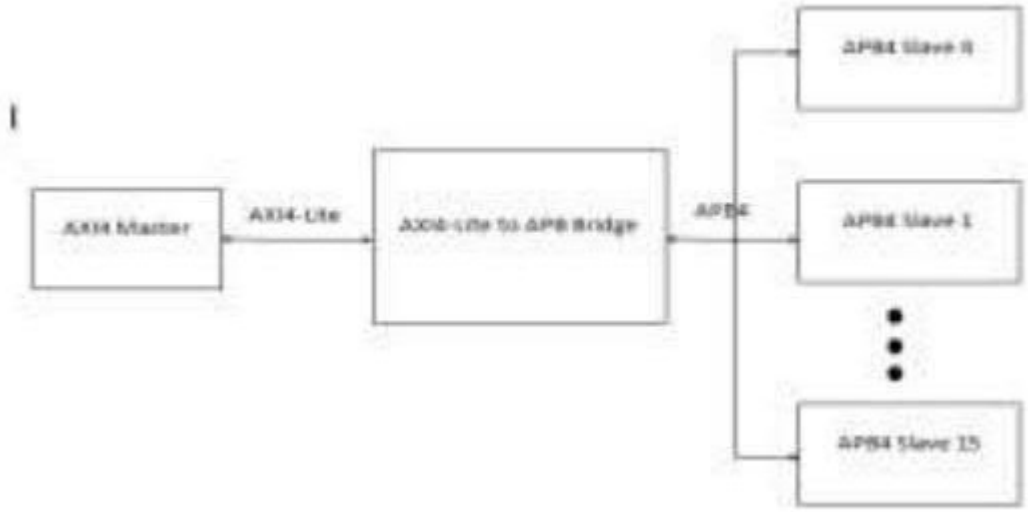
Block Diagram The AXI4-Lite to APB Bridge provides an interface between the high-performance AXI domain and the low power APB domain. It appears as a slave on AXI bus but as a master on APB that can access up to sixteen slave peripherals. Read and write transfers on the AXI bus are converted into corresponding transfers on the APB. The AXI4-Lite to APB bridge Block diagram is shown in Figure1



Features of bridge The Xilinx AXI to APB Bridge is a soft IP core with these features: 1. AXI interface is based on the AXI4-Lite specification 2. APB interface is based on the APB3 specification, supports optional APB4 selection 3. Supports 1:1 (AXI:APB) synchronous clock ratio 4. Connects as a 32-bit slave on 32-bit AXI4-Lite 5. Connects as a 32-bit master on 32-bit APB3/APB4 6. Supports optional data phase time out. 3.1.1 AXI4-Lite Slave Interface The AXI4-Lite Slave Interface module provides a bi-directional slave interface to the AXI. The AXI address and data bus widths are always fixed to 32-bits and 1024bits. When both write and read transfers are simultaneously requested on AXI4-Lite, the read request is given more priority than the write request. This module also contains the data phase time out logic for generating OK response on AXI interface when APB slave does not respond. 3.1.2 APB Master Interface The APB Master module provides the APB master interface on the APB. This interface can be APB3 or APB4, which can be selected by setting the generic C_M_APB_PROTOCOL. When C_M_APB_PROTOCOL=apb4, the M_APB_PSTRB, and M_APB_PPROT signals are driven at the APB Interface. The APB address and data bus widths are fixed to 32-bits.

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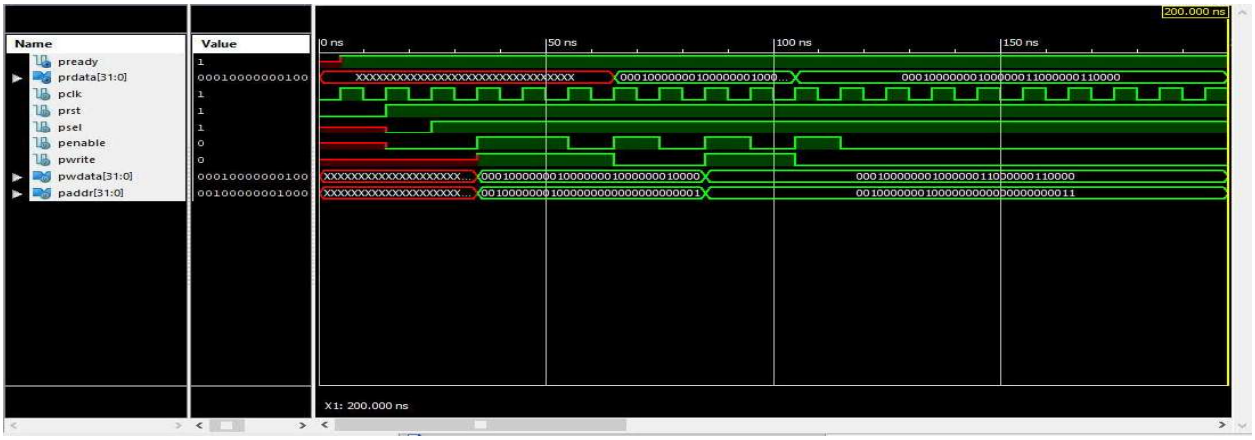
PROBLEM STATEMENT

In this brief, we have done the survey of different on-chip protocols along with their features and architectures. A descriptive comparison between various on-chip protocols is needed. So we have to find out the efficient protocol as it can efficiently transfers block of data thereby reducing the hardware resources and minimal power consumption. This can be verified by implementing the our projected protocol at RTL in HDL and comparing the same with other protocols by considering various parameters such as transfer time consumption, wire efficiency, valid data bandwidth, dynamic energy efficiency and power consumption.

SIMULATION RESULTS AND DESCRIPTION



CONCLUSION

This paper provides in detail the outline of the AMBA bus architecture and APB protocol in detail. According to the above mentioned specification, APB is designed and verified using XILINX 14.7 ISE. Here we summarized the six test cases, single and multiple write transaction with and without wait, multiple write transaction with and without wait states, multiple read and write transaction with and without wait. Hence the system is functionally correct. XILINX 14.7 ISE also ensures the functional correctness of the design. A detailed comparison has been done in between APB Bridge compatible with AMBA Specification (Rev 2.0) and APB Bridge compatible with AMBA 3 APB Specification . Also comparison between APB Bridge for UART application with and without data security has been done.

REFERENCES

- [1] ARM, "AMBA Specification Overview", http://www.arm.com/.
- [2]APB Example-AMBA system, Technical reference manual,ARM Inc.,1999.
- [3] Akhilesh Kumar, Richa Sinha, "Design and Verification analysis of APB3 Protocol with Coverage," IJAET, Nov 2011.
- [4] SanthiPriyaSarekokku, K. Rajasekhar, "Design and Implementation of APB Bridge based on AMBA AXI 4.0," IJERT, Vol.1, Issue 9, Nov 2012.
- [5] VERILOG Reference Manual, http://www.accellera.com
- [6] Samir Palnitkar, "Verilog HDL: A guide to Digital Design and Synthesis (2nd Edition), Pearson, 2008.

key components of Arithmetic and logic units, Digital signal processing blocks and Multiplier and accumulate units, determine the performance and throughput of the applications. Vedic Multiplier has become highly popular as a faster method for computation and analysis. They have found immense use in applications of image processing to save time and area. Image processing is the application of certain operations on images such as image sharpening, pattern recognition, edge detection etc, to extract some useful information from them or to enhance a particular feature in it. Hence it is essential in fields of mapping, holography, x-ray imaging, medical image processing and robotics. Similarly Digital Signal Processing is another area where high speed and low area Vedic Multipliers, are replacing commonly used conventional multipliers. Their importance couldn't have been more significant in the Semiconductor market demanding Digital Signal Processors for areas of wireless communication, audio and video processing, industrial control and portable electronics. The applications are as follows:

As the technology is scaling down, chip density is increasing so that millions of transistors are embedded on a single die. The yield may decrease due to process variations, deviation in parameters and lithographic effects [1- 3]. This advanced microelectronic technologies more susceptible to faults [4]. The response of a circuit may be invalid because of presence of faults [5-8]. This leads to inaccurate results. Fault secure systems are very much needed to withstand faults [9- 10]. So the self checking and repairing is necessary for correct operation of the circuit. In self checking the fault is detected by circuit itself and in self repairing the circuit can repair itself and produces correct output [11]. The overall circuit performance depends on individual gates of the circuit. Using small number of gates for design can increase the performance in terms of delay, area and power.

LITERATURE SURVEY: -

Anurupyena is a Nikhilam sutra's sub-sutra. The shortcut methods for multiplying numbers are provided. A new Vedic hybrid multiplier combining Karatsuba and Urdhava Tiryagbhyam algorithms has been developed. A new algorithm based on Nikhilam sutra was suggested with the bit reduction technique. A generic architecture was generally proposed for the Nikhilam sutra. the Anurupyena method is used only when the multiplicands are in the same range in mental calculations

Akbar, Muhammad Ali & Lee, Jeong A. (2014) [1] proposed an area-efficient self-repairing adder that can repair multiple faults and identify the particular faulty full adder. Fault detection and recovery has been carried out using self-checking full adders that can diagnose the fault based on internal

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functionality, independent of a fault propagated through carry. The idea was motivated by the common design problem of fault propagation due to carry in various approaches by self-checking adders. Such a fault can create problems in detecting the particular faulty full adder, and we need to replace the entire adder when an error is detected. We apply our self-checking full adder to a carry-select adder (CSeA) and show that the resulting self-checking CSeA consumes 15% less area compared to the previously proposed self-checking CSeA approach without fault localization. After observing fault localization with reduced area overhead, we utilize the self-checking full adder in constructing a self-repairing adder. It has been observed that our proposed self-repairing 16-bit adder can handle up to four faults effectively, with an 80% probability of error recovery compared to triple modular redundancy, which can handle only a single fault at a time.

Pankaj kumar, Rajendra Kumar Sharma proposed a complex computing system, processing units are dealing with devices of smaller size, which are sensitive to the transient faults. A transient fault occurs in a circuit caused by the electromagnetic noises, cosmic rays, crosstalk and power supply noise. It is very difficult to detect these faults during offline testing. Hence an area efficient fault tolerant full adder for testing and repairing of transient and permanent faults occurred in single and multi-net is proposed. Additionally, the proposed architecture can also detect and repair permanent faults. This design incurs much lower hardware overheads relative to the traditional hardware architecture. In addition to this, proposed design also provides higher error detection and correction efficiency when compared to the existing designs.

SIMULATION RESULTS AND DESCRIPTION

The below figure shows the output of the anurupena Vedic multiplier. Where schematic diagram and output waveforms of the anurupena Vedic multiplier is studied using Xylinx ISE 14.7 Software.

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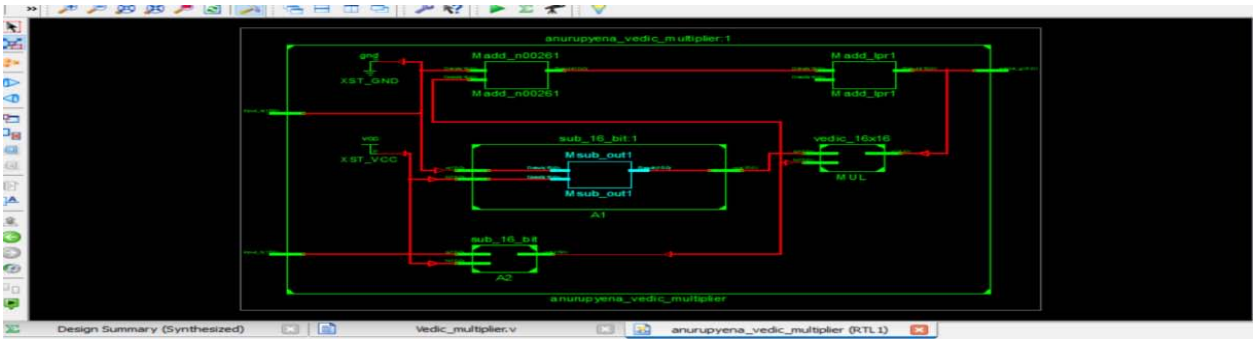

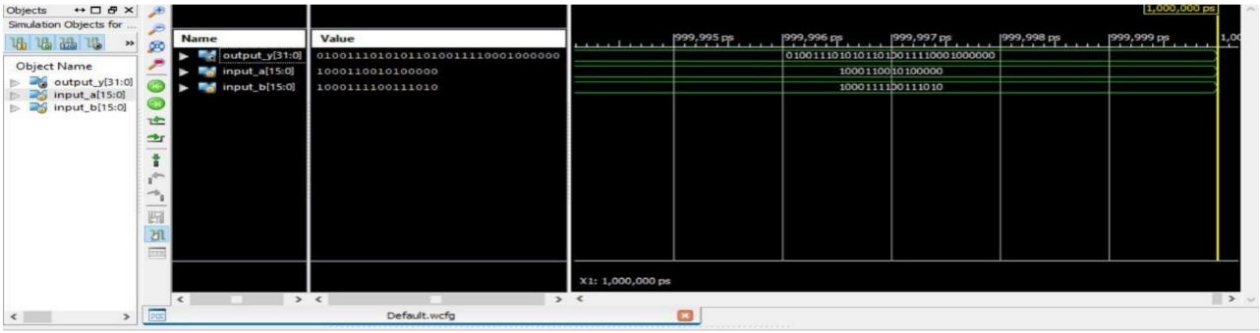

Here the input and output waveforms of anurupena vedic multiplier are studied and verified.

CONCLUSION

This paper presents a highly efficient method of multiplication – "Anurupyena Sutra" based on Vedic mathematics. Anurupyena is a sub-sutra in nikhalam sutra. It is a method for hierarchical multiplier design which clearly indicates the computational advantages offered by Vedic methods. Designed and simulated the code on Xilinx 14.7. The computational path delay and logic delay for proposed 16x16 bit Vedic multiplier is found to be 11 ns. It is observed that the Vedic multiplier is much more efficient than Array and Booth multiplier in terms of execution time (speed). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education.

REFERENCE

- Moss D J M, Boland D and Leong P H W 2019 A two-speed, Radix-4, serial–parallel multiplier. IEEE Trans. Very Large Scale Integr. (VLSI) Systems 27: 769–777
- Krizhevsky A, Sutskever I and Hinton G E 2012 ImageNet classification with deep convolutional neural networks. In: Proceedings of the 25th International Conference on Neural Information Processing Systems, pp. 1097–1105

- Lecun Y, Bottou L, Bengio L and Haffner P 1998 Gradientbased learning applied to document recognition. Proceedings of the IEEE 2278–2324
- Han S, Pool J, Tran J and Dally D J 2015 Learning both weights and connections for efficient neural networks. In: Proceedings of the. 28th International Conference on Neural Information Processing Systems, pp. 1135–1143
- Manikandan S K and Palanisamy C 2016 Design of an efficient binary Vedic multiplier for high speed applications using Vedic mathematics with bit reduction techniques. Circuits Syst. 07: 2593–2602
- Manikandan S K and Palanisamy C 2016 Design of high speed Vedic multiplier based on Nikhilam sutra algorithm using successive approximation. Asian J. Res.Soc. Sci. Hum. 6: 608
- Nisha Angeline M and Valarmathy R S 2016 Implementation of N-bit binary multiplication using N–1 bit multiplication based on Nikhilam sutra and Karatsuba principles using complement method. Circuits Syst. 7: 2332–2338
- Nisha Angeline M and Valarmathy R S 2016 Implementation of hybrid Vedic multiplier using Nikhilam sutra and Karatsuba algorithm for N-bit multiplier using successive approximation of N–1 bit multiplier. Asian J. Inf. Technol. 15: 3598–3604
- Nisha Angeline M and Valarmathy R S 2016 Implementation of N-bit binary multiplication using N–1 bit multiplication based on Nikhilam sutra principles and bit reduction. Trans. Rev. 7: 982–992

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INTELLEGENT AMBULANCE FOR CITY TRAFFIC POLICE

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ABSTRACT

The accretion of traffic has led to the use of more sophisticated Traffic management system in today's society. Traffic Congestion is a major factor which forestalls the smooth flow of Ambulance vehicles. To abate the inconvenience caused by the traffic, the Traffic Light Controller (TLC) is used which minimizes the waiting time of vehicle and also manages traffic load. RF based systems play a crucial role in solving the problems caused by traffic. The project is a replica of a two way lane crossing of real time scenario. In the first part, concentrated on problems faced by Ambulances, RF concept is used to make the Ambulance's lane Green and thus provides a free way without interrupting the Ambulance. In the second part, concentrated on problems faced by Priority vehicles, RF transmitter and receiver are used to provide dynamic traffic control and thus increasing the duration of the Green light of the lane in which traffic density is high and hence, regulating traffic.

Hardware requirement:

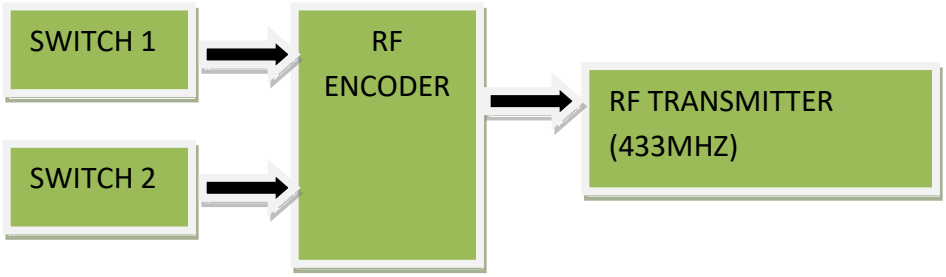
- Arduino nano
- RF transceiver module
- Led's(traffic lights)

Software requirement:

- Arduino IDE
- Embedded C

Block diagram:

TX:



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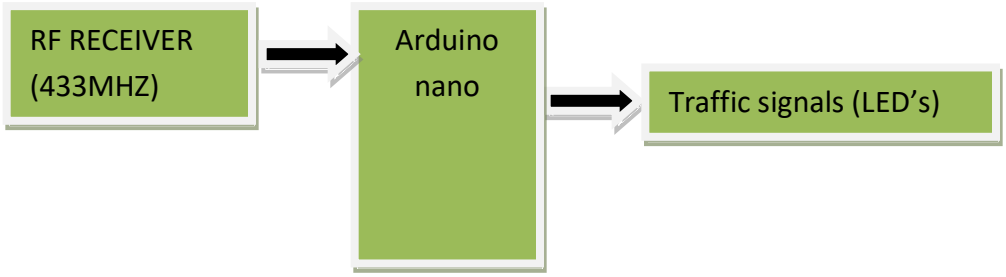
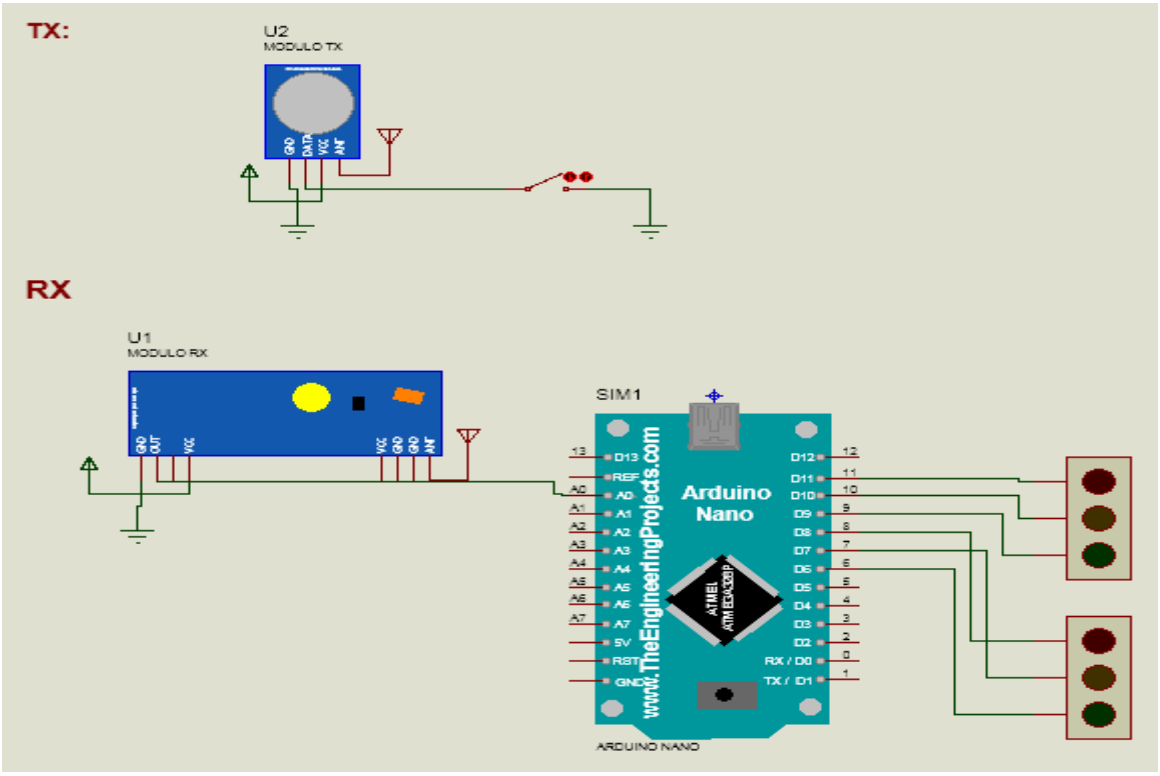


CIRCUIT DIAGRAM:



WORKING PRINCIPLE:

When the ambulance at emergency comes to any traffic post the traffic signals automatically stop the signals and give green signal for this ambulance.

The ambulance carries an RF transmitter and every traffic post will have an RF receiver. So whenever the ambulance comes near the traffic, the ambulance will transmit a code say "emergency" the receiver will receive this signal and check in the database of the micro controller. Then it immediately switch off the other signals that is it make all the signals red and later make this particular direction signal green. So by doing this the ambulance can go without any problem.

ADVANTAGES

Advantages of Smart Ambulance System:

1. Ambulance service will no longer be affected by traffic jams.

2. Use of radio frequency signal (not blocked by objects, fast).

3. Over a wide range applicability.

4. One time investment cost.

5. Life of people can be saved.

Advantages of Traffic Density Control System:

1. A modernized way of controlling traffic.

2. Number of road accidents can be reduced to a large extent.

3. Easy traffic regulation in busy cities such as Delhi, Mumbai etc..

4. Help the traffic police in easy control of traffic

CONCLUSION

This Project which demonstrates an automated patient monitoring system has its own merits which are discussed above. We have presented some applications of how people could benefit from living in homes that have wireless sensor technologies for improving the quality of life. The first decade of research in the field of wearable technology was marked by an emphasis on the engineering work needed to develop wearable sensors and systems, recent studies have been focused on the application of such technology toward monitoring health and wellness. This consideration was the basis for this project review. This project summarized enabling technologies developed over the past decade and put a great deal of emphasis on surveying studies focused on the deployment of wearable sensors and systems in the context of a concrete clinical applications, with main focus on rehabilitation.This wearable module can transmit the data continuously over a fiber optic link or through an internet digital radio. The received data can be stored in separate memory and be processed by a microcontroller.

FUTURE SCOPE

- This project can be enhanced in such away as to control automatically the signals depending on the traffic density on the roads using sensors like IR detector/receiver module extended with automatic turn off when no vehicles are running on any side of the road which helps in power consumption saving.

- No. of passing vehicle in the fixed time slot on the road decide the density range of traffics and on the basis of vehicle count microcontroller decide the traffic light delays for next recording interval. In future this system can be used to inform people about different places traffic

condition. This can be done through RADIO. Data transfer between the microcontroller and computer can also be done through telephone network, data call activated SIM This technique allows the operator to gather the recorded data from a far end to his home computer without going there

- Traffic lights can be increased to N number and traffic light control can be done for whole city by sitting on a single place.

- In ambulance system, the data of the patient in the ambulance can be sent to the Hospitals via GSM technology. Thus, it can provide early and fast treatment of the patient.

REFERENCES

[1]. Legon-Okponglo, "Design and development of microcontroller based traffic system using image processing techniques". University of Ghana, published in ICAST, 2012 IEEE 4th International Conference.

[2]. Amrita Rai and Govind Singh Patel Multiple Traffic Control Using Wireless Sensor and Density Measuring Camera. Sensors & Transducers Journal Vol. 94, Issue 7, July 2008, pp. 126-132.

[3]. Muhammad Ridwan. "Development of a Low Cost Smart Traffic Controller System". Department of Mechanical and Materials Engineering Faculty of Engineering and Built Environment University Kebangsaan Malaysia, 43600 Bangi Selangor, Malaysia.

[4]. "Highway traffic model-based density estimation"-IEEE paper by Morarescu, Nancy Univ., France, published in American Control Conference(ACC), 2011.

[5]. W. Wen & C.L. Yang. "A dynamic and automatic traffic light control system for solving the road congestion problem".

[6]. "Iterative learning based Freeway density control"-IEEE paper by Jianye Li, Wuyi Univ.,China, published in Information Engineering and Computer Science(IECS),2nd International Conference

[7].http://www.edgefxkits.in/embedded/pic/density-based-traffic-signal-system-using-picmicrocontroller.

[8].http://www.ijater.com/Files/IJATsER_03_06.pdf

[9] Muhammad Ridwan. "Development of a Low Cost Smart Traffic Controller System". Department of Mechanical and Materials Engineering Faculty of Engineering and Built Environment University Kebangsaan Malaysia, 43600 Bangi Selangor, Malaysia.

[10] Marco Wiering. "Intelligent Traffic Light Control". Institute of information and computing sciences, Utrecht University

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AREVIEWONFAULTTOLERANTREVERSIBLEFULLADDERDESIGNUSING GATEDIFFUSIONINPUT

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Abstract

GDI technique allows minimization of area and power consumption of digital circuits. Thereversible gate preserves same parity between output and input vectors is called fault tolerant but thedimension should be 3. In this design, Peres Gate is designed using Gate Diffusion Input using 8transistors. The proposed new Peres Gate is used to design full adder with power efficient and faulttolerant. In this work power consumption 51.62µW is achieved for supply voltage 1V and the total areais492µm2 .TheschematicisdesignedinDSCH 2 andlayoutisdoneinMicrowind 2.

Keywords

PeresGate,ReversibleLogicGate,LowPower,GateDiffusionInput(GDI),Fulladder,120nmTechnology,Microwind2,DSCH2.

INTRODUCTION

In VLSI digital circuits, power and area reduction is the important parameter which decides theefficiencyofthecircuit[1][4].Powerconsumptionistheprimaryfactorinhighperformancecomputingapplication,Imageprocessingapplications.TheauthorR.Landauerhassaidthattocomputeirreversiblelogic,kTln2 joulesofheatenergygeneratesperbitinformation lost[2].

Theusualdigitalcomputerprogramfrequentlyperformsoperationsthatseemtothrowawayinformation about the computer's history, leaving the machine in a state whose immediate predecessoris ambiguous. Such operations include erasure or overwriting of data, and entry into a portion of theprogram addressed by several different transfer instructions. In other words, the typical computer islogically irreversible - its transition function (the partial function that maps each whole-machine stateonto its successor, if the state has a successor) lacks a single-valued inverse. Landauer [I] has posed thequestion of whether logical irreversibility is an unavoidable feature of useful computers, arguing that itis, and has demonstrated the physical and philosophical importance of this question by showing thatwhenever a physical computer throws away information about its previous state it must generate acorrespondingamountofentropy.Therefore,acomputermustdissipateatleastkTln2ofenergy

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(about 3 X 10"' joule at room temperature) for each bit of information it erases or otherwise throwsaway. An irreversible computer can always be made reversible by having it save all the information itwouldotherwisethrowaway.

For example, the machine might be given an extra tape (initially blank) on which it could record eachoperation as it was being performed, in sufficient detail that the preceding state would be uniquelydetermined by the present state and the last record on the tape. However, as Landauer pointed out, thiswouldmerely postpone the problem of throwingaway unwantedinformation,since the tape wouldhave to be erased before it could be reused. It is therefore reasonable to demand of a useful reversiblecomputer that, if it halts, it should have erased all its intermediate results, leaving behind only thedesired output and the originally furnished input. (The machine must be allowed to save its input- otherwise itcould notbe reversible and still carry outcomputations in which the inputwas notuniquely determined by the output.) We will show that general-purpose reversible computers (Turingmachines)satisfyingtheserequirementsindeedexist,andthattheyneednotbemuchmorecomplicated than the irreversible computers on which they are patterned. Computations on a reversiblecomputer take about twice as many steps as on an ordinary one and may require a large amount oftemporary storage. Before proceeding with the formal demonstration, the argument will be carriedthroughatthe presentheuristiclevel.

LITERATUREWORK

R.Landauer,[2]hasproposed“IrreversibilityandHeatGenerationintheComputationalProcess”,Inrecentstudies,reversiblelogichasemergedasagreatsceneofresearch,havingapplicationsinlowpowerCMOScircuits,opticalcomputing,quantumcomputingandnanotechnology. The classical logic gates such as AND, OR, EXOR and EXNOR are not reversible. Inthe existing literature, reversible sequential circuits designs are offered thatare improved for thenumberof thegarbageoutputsandreversiblegates.Minimizingthenumberof garbageisverynoticeable. In the present paper, we show a design of the reversible comparator based on the quantumgates implementation of the reversible DG gate. The reversible DG gate is designed by using 3 × 3quantum gates such as NOT, CNOT, Controlled-V and Controlled-V+ gates. Also, we have used theTR gate andvarious types of quantum gates in the implementation results.Low power three-bitcomparator is designed using DG Gate, New Gate and Fredkin Gate. In order to evaluate the benefit ofusing the DG gate proposed in this paper, one-bitcomparator is constructed. The design is useful forthefuturecomputingtechniques likequantumcomputers.Theproposeddesignsareimplementedusing

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VHDLandfunctionallyinvestigatedusingQuartusIIsimulator.

C.HBennett[3]"Logical Reversibility ofcomputations" Basedonbipolardynamiclogic(BDL) and bipolar quantum linear algebra (BQLA) this work introduces bipolar quantum logic gatesand quantum cellular combinatorics with a logical interpretation to quantum entanglement. It is shownthat: 1) BDL leads to logically definable causality and generic particle-antiparticle bipolar quantumentanglement;2)BQLAmakescompositeatom-atombipolarquantumentanglementreachable.Certain logical equivalence is identified between the new interpretation and established ones. A logicalreversibility theorem is presented for ubiquitous quantum computing. Physical reversibility is brieflydiscussed. It is shown that a bipolar matrix can be either a modular generalization of a quantum logicgate matrix or a cellular connectivity matrix. Based on this observation, a scalable graph theory ofquantum cellular combinatorics is proposed. It is contended that this work constitutes an equilibrium-based logical extension to Bohr's particle-wave complementarity principle, Bohm's wave function andBell's theorem. In the meantime, it is suggested that the result may also serve as a resolution, ratherthan a falsification, to the EPR paradox and, therefore, a equilibrium-based logical unification of localrealismandquantumnon-locality.

PROPOSEDWORK

To ensure all the digital devices be more efficiently working by designing in way that thespeed is high and power is conserved by scaling down power dissipation. Slower operation in PTLdue to reduced current drive. Due to direct path static power consumption will increase, it leads tolatchup problems and in CMOS technology the numbers of transistors are required more. Sloweroperation in PTL due to reduced current drive. Due to direct path static power consumption willincrease, it leads to latchup problems and in CMOS technology the numbers of transistors arerequired more. To overcome this problem, the Gate Diffusion Input technique is proposed reducenumberswitchingactivitiesaswellaspowerconsumption.TheGDItechniqueuseslessnumberof transistors and reduces the area. In this design, we have designed Peres gate using Gate InputDiffusion using 8 transistors is shown in fig.6.The proposed new Peres gate is used to design fulladder with power efficient and fault tolerant using reversible logic gates is shown in fig.7. In thisdesign first we have designed 3T XOR gate and 2T AND gate [1]. Peres gate is also comes underparity preserving reversible gates because it satisfy the following equation (4) and feedbacks, fanoutsarenotallowedinthisreversiblelogic.

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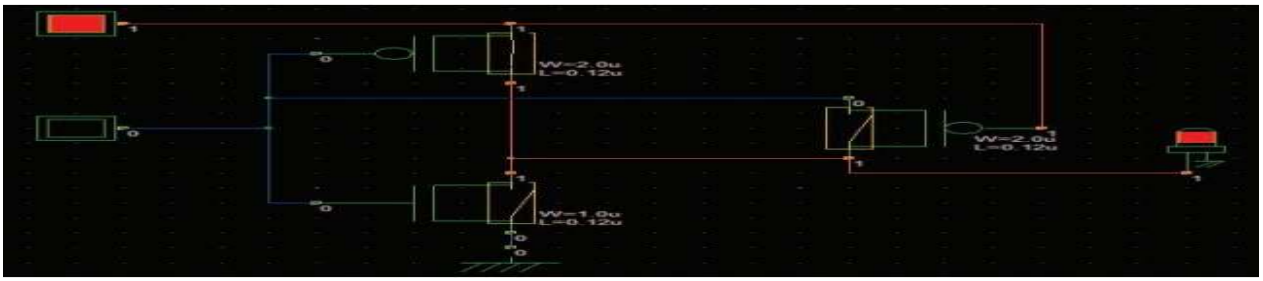
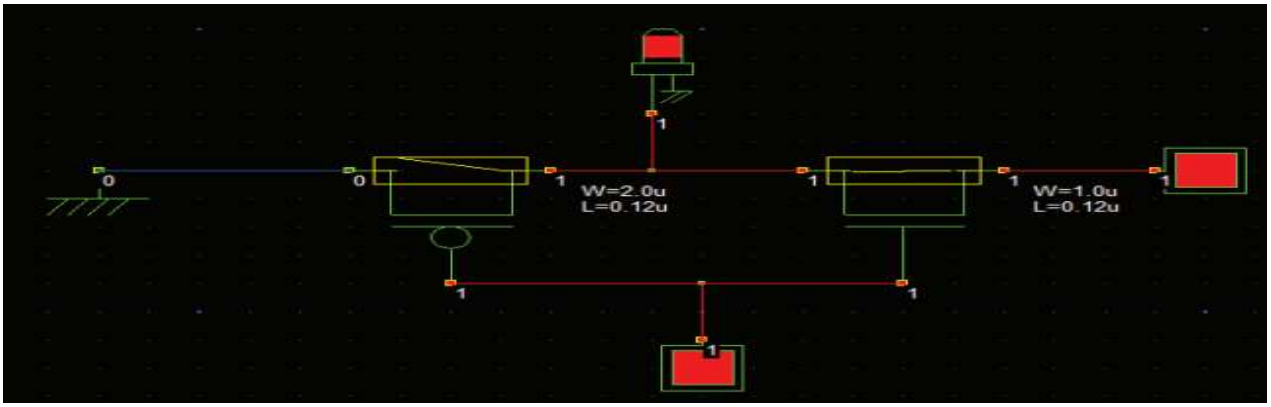
$$A \oplus B \oplus C = P \oplus Q \oplus R$$

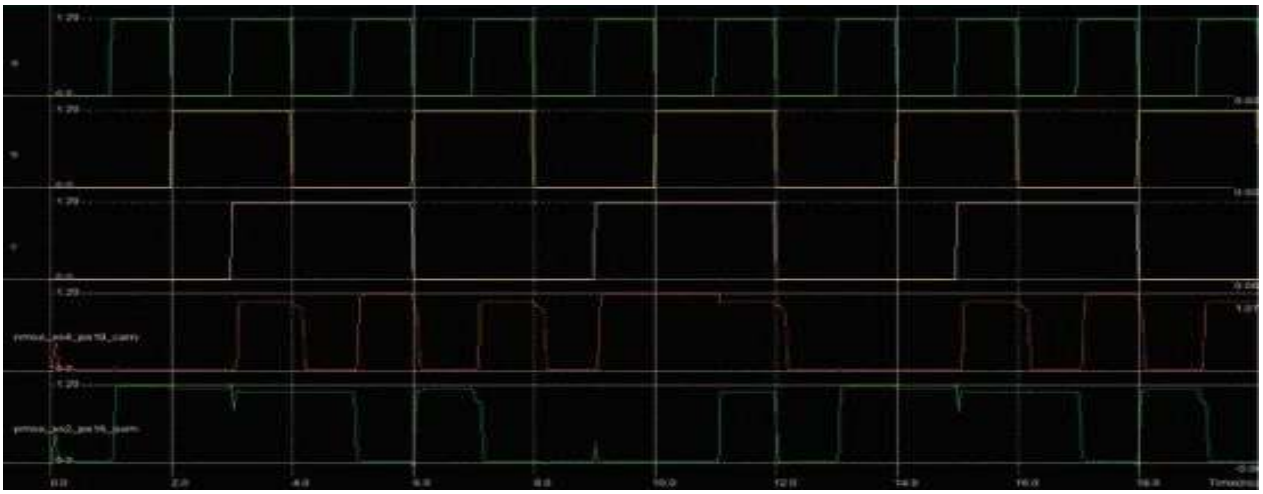


3TXORgateusingGDItechnology[1]



2TANDgateusingGDItechnology

RESULTS



Simulationresultswithsupplyvoltage 1.2V

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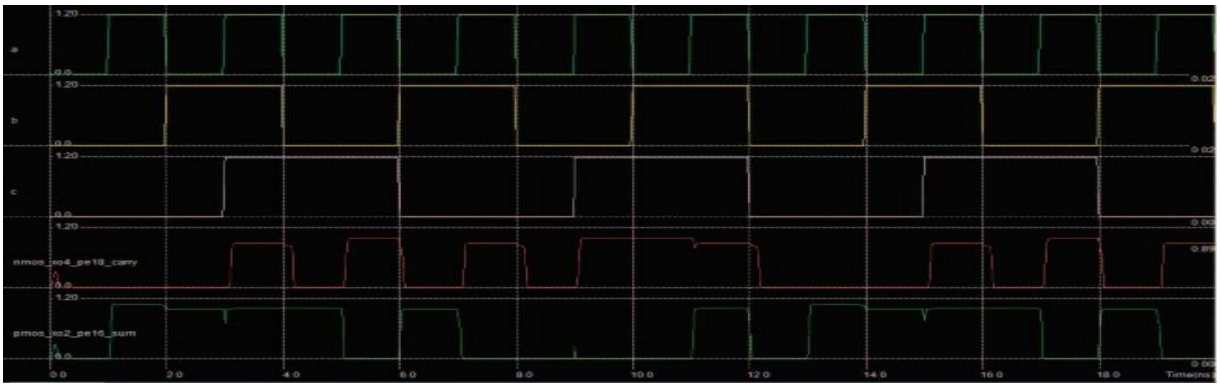
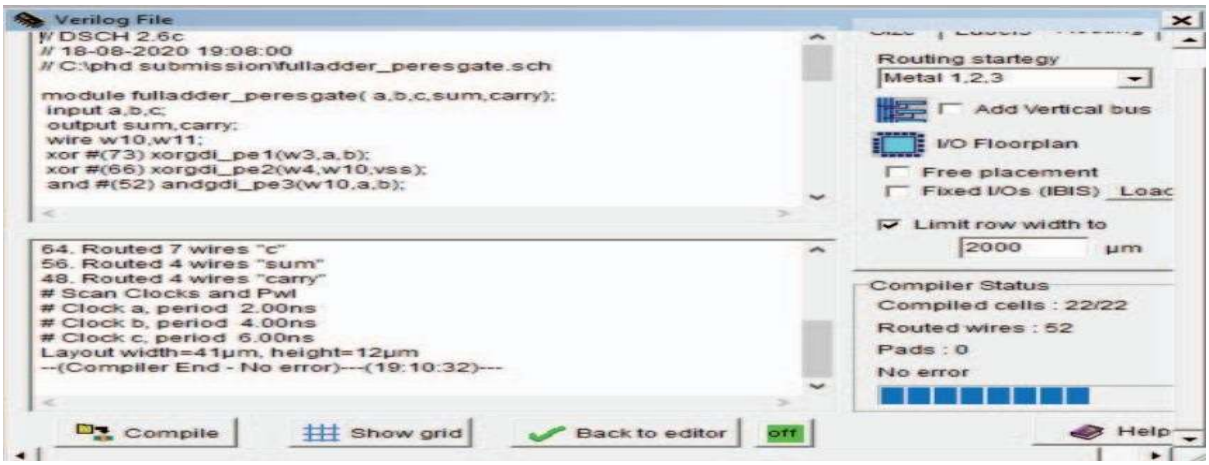


Simulationresultswithsupplyvoltage 1.0V



Areaanalysis layoutwidth=41µmandlength=12µm

CONCLUSION

In this design, Peres Gate is designed using Gate Diffusion Input using 8 transistors. The proposed newPeres Gate is used to design full adder with power efficient and fault tolerant. In this work powerconsumption51.62µW isachievedforsupplyvoltage 1V andthetotalareais492µm2.

REFERENCES

[1] SomashekharMalipatil,VikasMaheshwari,andMarepallyBhanuChandra,"AreaOptimization ofCMOSFullAdderDesignUsing3TXOR",978-1-7281-5284-4/20/$31.00,2020IEEE.

[2] R.Landauer,"IrreversibilityandHeatGenerationintheComputationalProcess",IBMJournalofResearch andDevelopment,5,pp.183-191,1961

[3] C.HBennett"LogicalReversibilityofcomputations"IBMJ.Researchanddevelopment,pp525-

532,November1973.

[4] M.Alioto,Ultra-low powerVLSIcircuitdesign demystified and explained: a tutorial,IEEETransactionsonCircuits andSystems—PartI(invited)59(1)(2012).

[5] A. Morgenshtein et al., "Gate-diffusion input (GDI) - a technique for low power design of digitalcircuits: analysis and characterization," 2002 IEEE International Symposium on Circuits and Systems.Proceedings.

[6] A. Peres, “Reversible logic and quantum computers”, Physical Review: A, vol. 32, no. 6, pp. 3266-3276,1985.

[7] S. Hiremath, A. Mathad, A. Hosur and D. Koppad, "Design of low power standard cells using fullswing gate diffusion input," 2017 International Conference On Smart Technologies For Smart Nation(SmartTechCon),Bangalore,2017,pp.940-945,doi: 10.1109/SmartTechCon.2017.8358510.

[8] Md. Saiful Islam et al., “Synthesis of Fault Tolerant Reversible Logic Circuits”, 978-1-4244-2587-7/09/$25.00©2009IEEE.

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A REVIEW ON PARALLEL CMOS IMPLEMENTATION OF NOR LOGIC IN BOTH PULL-UP AND PULL-DOWN NETWORKS

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ABSTRACT

New advancements in CMOS IC fabrication technology allow for chips with extremely tiny feature sizes, resulting in much smaller ICs with much higher clock rates. Although higher clock rates make synchronous logic designs faster, they also increase power consumption and cause many clock distribution issues. Asynchronous clockless logic design paradigms have recently been considered as a solution for these ever- increasing clock issues. Aware to that the implementation of CMOS logic based on NAND and NOR logic principles of pull-up and pull-down combination of transistors, this work shows how by using both the combinations of pull-up and pull-down transistors in parallel too we can realize a NOR logic. This is illustrated with the help of using DSCH software and studied under microwind software in terms of both area and timing signals.

Index Terms- CMOS, NOR, Pull-up, Pull-down, Parallel and DSCH software.

INTRODUCTION

There are three basic backgrounds of electronics which are analog electronics, digital electronics and communication. With the medium of a flow chart I will depict how electronics and communication engineering works realistically and how this algorithm is necessary for understanding the field of electronics and communication engineering.

FUNDAMENTAL BLOCKS OF ELECTRONICS AND COMMUNICATION

There are two basic fundamental blocks as everyone knows i.e.

1. ELECTRONICS
   - Analog Electronics
   - Digital Electronics
2. COMMUNICATION
   - Analog Communication
   - Digital Communication

Preference to analog electronics is the basic fundamental engineering step towards electronics and communication as its provides us an idea how basic circuit designing using verily visible physical analog

components is accomplished further providing the basic background of understanding op- amps and necessity of digital electronics. Analog device and their circuits such as diode, transistors: BJTs, FETs are majorly used in analog electronics as the key analog elements supported by various simple and compound networks. Major circuit works which required major analog device/ devices and their associated networks as stated above would be easily performed by using a single Op- amp IC, thus reducing the amount number of analog devices, their possible networks and also the size of the circuit. No doubly Op- amp has eased the circuit designing but it was limited to a certain extent, this extent was been able to extended and bounded as per our needs with the help of digital electronic leading to design dense integrated circuits using CAD tools and ultimately leading to VLSI technology.

Lately, the rapid advance in multimedia and digital communication systems, real time signal processing like audio signal processing, image and video processing are heavily needed. Many applications such as Processors and Digital Signal Processing operations such as Filtering, Convolutional transformation, require some form of addition such as multiplication, multiply and accumulate operation (MAC) and subtraction. The 1-bit full adder cell is the main block in all these modules [1]. Because of the need in portable devices such as laptop and cell phones for low power consumption. The power consumption, small area and high speed are the crucial factors to be considered in VLSI design with high performance [2]. There were many techniques to design in VLSI circuit and minimize the power and area, but their best gate diffusion input The CMOS designing/ design constitute a pull-up and a pull-down network with:

1. Pull-up network having only PMOS transistors
2. Pull-down network having only NMOS transistors.

LITERATURE SURVEY

The design considerations for a simple inverter circuit were presented in the previous chapter. In this chapter, the design of the inverter will be extended to address the synthesis of arbitrary digital gates such as NOR, NAND and XOR. The focus will be on combinational logic (or non-regenerative) circuits that havethe property that at any point in time, the output of the circuit is related to its current input signals by some Boolean expression (assuming that the transients through the logic gates have settled). No intentional connection between outputs and inputs is present. In another class of circuits, known as sequential or regenerative circuits —to be discussed in a later chapter—, the output is not only a function of the current input data, but also of previous values of the input signals (Figure 6.1). This is accomplished by connecting one or more outputs intentionally back to some inputs. Consequently, the circuit “remembers” past events and has a sense of history. A sequential circuit includes a combinational logic portion and a module that holds the state. Example circuits are registers, counters, oscillators, and memory.

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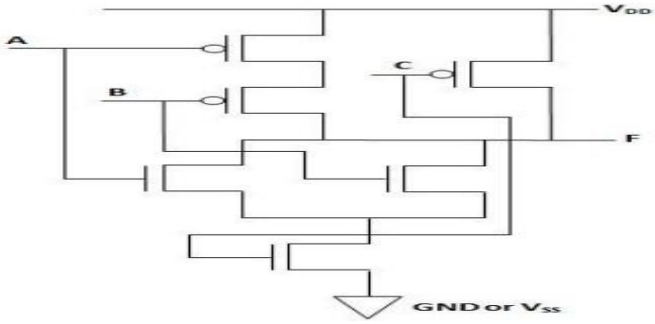
Design and Simulation of CMOS function by H. Abdul Wasay has (International Research Journal of Engineering and Technology (IRJET)) Proposed Implementing the function using CMOS logic i.e. pull- up and pull- down combination and testing the implemented transistor based logical circuit using DSCH software aid. Here the function has three input variables i.e. A, B and C respectively. The function with a output F has A and B in NOR logic with along with them in NAND logic. Designing them with the fundamental of CMOS design topology.



CMOS circuit for the function $F = \overline{(A + B)C}$

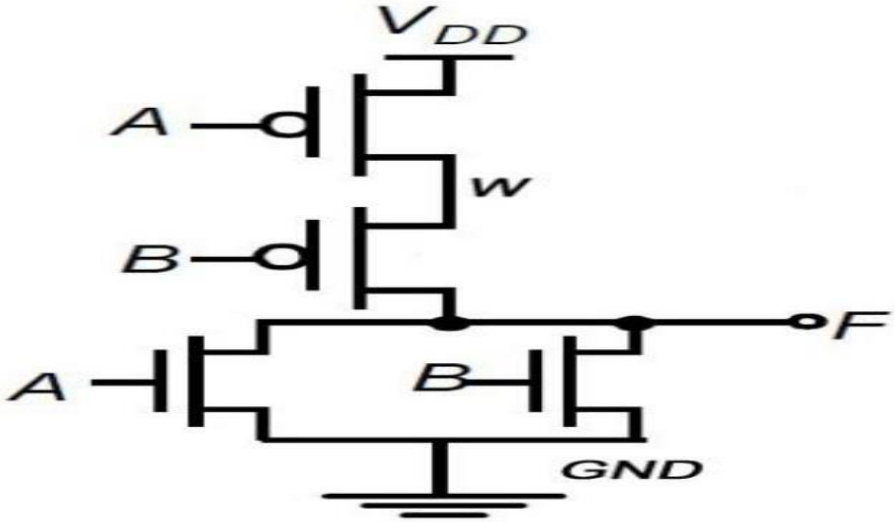
EXISTING METHOD

BASIC NOR LOGIC PULL-UP AND PULL-DOWN NETWORKS

A. A basic NOR logic as per the CMOS design topology follows:

PUN- PMOS transistors- series Connection

PDN- NMOS transistors-Parallel Connection



Two input CMOS based NOR Gate

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Input A	Input B	Output F
0	0	1
0	1	0
1	0	0
1	1	0

Table. 2.0 – Truth Table of Two input CMOS based NOR Gate

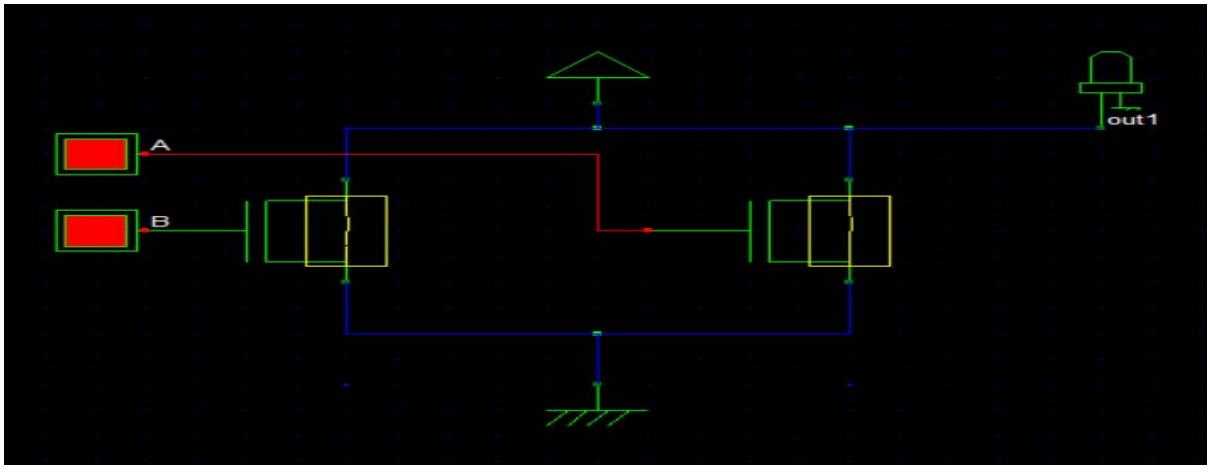
The basic NOR logic verifies the NOR truth table. Implementing the basic NOR logic using DSCH software, it is observed to the conclusive verification of the NOR logic. ¬ Pull-up and pull-down arrangement.

SIMULATION RESULTS AND COMPARISON

OBSERVATION/ ANAYLSIS ON DSCH CAD The implementation of the NOR logic as done using DSCH software is been conclusively verifying all the possible logical combinations. The observation obtained is same for the fundamental/ basic CMOS design topology and for the parallel transistors implementation in both pull-up and pull-down networks.

The CMOS circuit thus designed is implemented using DSCH software and the observance on the transistor switching behavior can also be seen for every input logical combination.

We can perform many control functions by connecting switches, or transistors, in series or parallel. In the example on the left below, we are using two NPN transistors in parallel to connect the output to ground, or *pass 0*. if either *X* or *Y* is one. The circuit on the right uses two PNP transistors in series to *pass* 1, if both *X* and *Y* are zero. Note that, when both circuits are receiving the same two inputs, exactly one will be passing a value.



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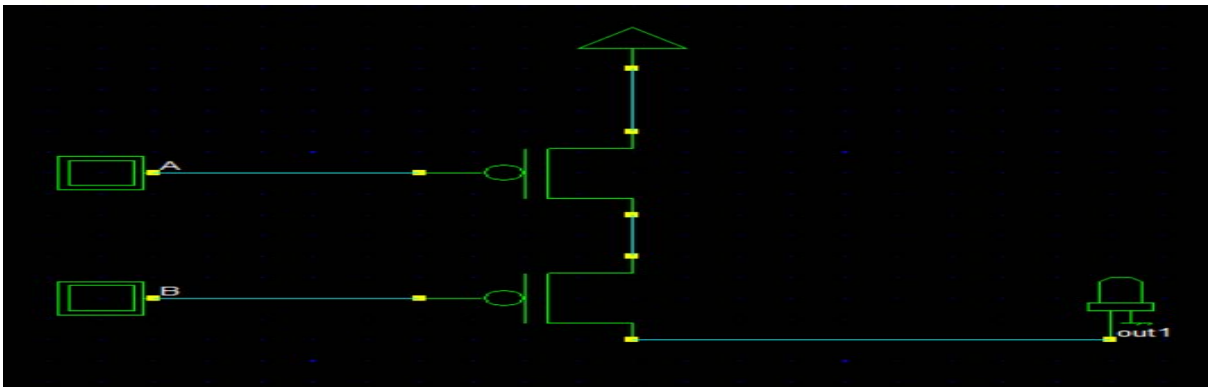

CONCLUSION

Such logic implementations may be futuristic for developments of different digital logic circuits and motivate towards the existence of further different network combinations.

It can be concluded that a CMOS NOR logic can be implemented by using the Pull-up PMOS transistors in parallel along with Pull-down NMOS transistors in parallel. The circuit is found to be ON in all the input configurations. Through this the switching behaviour of transistors at different inputs is observed, leading to coverage of digital integrated transmission paths in digital electronics.

REFERENCES

[1] Design and Simulation of CMOS function by H. Abdul Wasay (International Research Journal of Engineering and Technology (IRJET))

[2] Noor's Algorithmic Flow of Electronics and Communication Engineering by Noor Ul Abedin (International Research Journal of Engineering and Technology (IRJET))

[3] Digital Integrated Circuits- A design perspective2 nd Ed by Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic (PHI)

[4] Basic VLSI Systems and Circuits- 2 nd Ed by Kamran Eshraghian, Douglas A. Pucknell (PHI)

[5] Introduction to VLSI Circuits and Systems by John P. Uyemura- 2 nd Ed (Wiley India Pvt. Ltd.)

[6] Analog Integrated Cicuit Design by David A. Johns and Ken Martin- 2 nd Ed (Wiley India Pvt. Ltd.)

[7] VLSI Design by Partha Pratim Sahu (McGraw Hill)

[8] Design of Digital integrated circuits by David A. Hodges, Horace G Jackson- 3 rd Ed (McGraw Hill)

[9] Modern VLSI Design by Wayne Wolf- 4 th Ed (Pearson Education)

[10] VLSI Design by Shiva Kundarapu and Krishna Gimkala (PP).

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A REVIEW ON THE DESIGN OF LOW-POWER HIGH-PERFORMANCE 2-4 AND 4-16 MIXED-LOGIC LINE DECODERS.

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ABSTRACT

This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders are designed by using mixed-logic 2–4 predecoders combined with standard CMOS postdecoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative simulations shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

INTRODUCTION

STATIC cmos circuits are used for the vast majority of logic gates in integrated circuits [1]. They consist of complementary *N*-type metal-oxide-semiconductor (nMOS) pull down and P-type metal-oxide semiconduct r (pMOS) pullup networks and present good performance as well as resistance to noise and device variation. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. Pass transistor logic (PTL) was mainly developed in the 1990s, when various design styles were introduced [3]–[6], aiming to provide a viable alternative to CMOS logic and improve speed, power, and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates. Line decoders are fundamental circuits, widely used in the peripheral

circuitry of memory arrays (e.g., SRAM) [7]–[9]. This brief develops a mixed-logic methodology for their im- plementation, opting for improved performance compared to single-style design

EXISTING METHOD: CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. Pass-transistor logic was mainly developed in the 1990s, when various design styles were introduced [3-6], aiming to provide a viable alternative to CMOS logic and improve speed, power and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual Nmos / pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates.

PROPOSED METHOD: This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g. SRAM), multiplexing structures, implementation of boolean logic functions and other applications. Despite their importance, a relatively small amount of literature is dedicated to their optimization.

Applications: ¬ Automotive ¬ Portable and wireless ¬ Networking and telecommunications

Advantages: ¬ Area, delay, low power, noise immunity

LITERATURE REVIEW:

1.IN "I. Shin, J.-J. Kim, Y.-S. Lin, and Y. Shin, "A pipeline architecture with 1-cycle timing error correction for low voltage operations," in *Proc. IEEE Int. Symp. Low Power Electron. Design*, Sep. 2013, pp. 199–204."

We present a new timing error correction scheme which allows each pipeline stage to halt for one cycle only. The small timing penalty for the error correction operation in the proposed scheme makes it possible to eliminate the extra timing guardband that was needed to accommodate timing uncertainty due to process variations. As a result, lower supply voltage can be used with the proposed scheme for low power operations. Compared to the previous 1-cycle error correction scheme which uses two-phase transparent latch based pipeline [1], the proposed scheme can be applied to the pipeline based on

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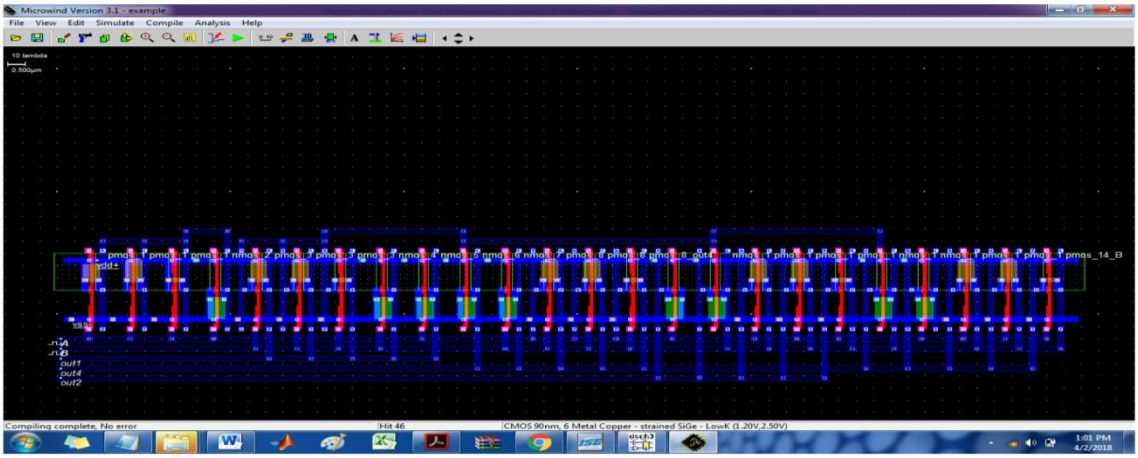

CONCLUSION

This brief has introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2–4 line decoder topologies, namely 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer reduced transistor count and improved powerdelay performance in relation to conventional CMOS decoders. Furthermore, four new 4–16 line decoder topologies were presented, namely 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, realized by using the mixed-logic 2-4 decoders as predecoding circuits, combined with postdecoders implemented in static CMOS to provide driving capability. A variety of comparative spice simulations was performed at 32 nm, verifying, in most cases, a definite advantage in favor of the proposed designs. The 2–4LP and 4–16LPI topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2–4LPI, 2–4HP, and 2–4HPI, as well as the corresponding 4–16 topologies (4–16LP, 4–16HPI, and 4–16HP), proved to be viable and all-around efficient designs; thus, they can effectively be used as building blocks in the design of larger decoders, multiplexers, and other combinational circuits of varying performance requirements. Moreover, the presented reduced transistor count and lowpower characteristics can benefit both bulk CMOS and SOI designs as well. The obtained circuits are to be implemented on layout level, making them suitable for standard cell libraries and RTL design.

REFERENCES

[1] N. H. E. Weste and D. M. Harris, CMOS VLSI Design, a Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley, 2011.

[2] R. Zimmermann and W. Fichtner, “Low-power logic styles: CMOS versus pass-transistor logic,” IEEE J. Solid State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[3] K. Yano et al., “A 3.8-ns CMOS 16 × 16-b multiplier using complementary pass-transistor logic,” IEEE J.

Solid-State Circuits, vol. 25, no. 2, pp. 388–393, Apr. 1990.

[4] M. Suzuki et al., "A 1.5 ns 32b CMOS ALU in double pass-transistor logic," in Proc. IEEE Int. Solid-State Circuits Conf., 1993, pp. 90–91.

[5] X. Wu, "Theory of transmission switches and its application to design of CMOS digital circuits," Int. J. Circuit Theory Appl., vol. 20, no. 4, pp. 349–356, 1992.

[6] V. G. Oklobdzija and B. Duchene, "Pass-transistor dual value logic for low-power CMOS," in Proc. Int. Symp. VLSI Technol., 1995, pp. 341–344.

[7] M. A. Turi and J. G. Delgado-Frias, "Decreasing energy consumption in address decoders by means of selective precharge schemes," Microelectron. J., vol. 40, no. 11, pp. 1590–1600, 2009.

[8] V. Bhatnagar, A. Chandani, and S. Pandey, "Optimization of row decoder for 128 × 128 6T SRAMs," in Proc. IEEE Int. Conf. VLSI-SATA, 2015, pp. 1–4.

[9] A. K. Mishra, D. P. Acharya, and P. K. Patra, "Novel design technique of address decoder for SRAM," Proc. IEEE ICACCCT, 2014, pp. 1032–1035.

[10] D. Markovic, B. Nikoli ´ c, and V. G. Oklobdžija, "A general method in syn- ´ thesis of pass-transistor circuits," Microelectron. J., vol. 31, pp. 991–998, 2000.

[11] [Online]. Available: http://ptm.asu.edu/

[12] N. Lotze and Y. Manoli, "A 62 mV 0.13 µm CMOS standard-cellbased design technique using Schmitt-trigger logic," IEEE J. Solid State Circuits, vol. 47, no. 1, pp. 47–60, Jan. 2012.

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CONTENT BASED IMAGE RETRIEVAL USING FEATURE EXTRACTION WITH MACHINE LEARNING

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ABSTRACT

The retrieval performance of a content-based image retrieval (CBIR) system is mainly influenced by the feature representations and similarity measures. Recently, deep learning develops rapidly and the deep features based on deep learning have been applied widely because it has been shown that the features have very strong generalization. This paper applies the original deep features generated by convolution neural network (CNN) to CBIR, and uses linear support victor machine (SVM) to train a hyerplane which can separate similar image pairs and dissimilar image pairs to a large degree with the help of image fusion. The input of the SVM in this paper is pair features which are assembled by pair of images: the query image and each test image in the image dataset. The test images then are ranked by the distance between the pair features and the trained hyperplane. Experiments show that our method can significantly improve the performance of CBIR for object image retrieval tasks.

Keywords

CBIR; CNN; SVM; feature representations; Image Fusion; similarity measures

INTRODUCTION

Image:

An image is a two-dimensional picture, which has a similar appearance to some subject usually a physical object or a person.

Image is a two-dimensional, such as a photograph, screen display, and as well as a three-dimensional, such as a statue. They may be captured by optical devices such as cameras, mirrors, lenses, telescopes, microscopes, etc. and natural objects and phenomena, such as the human eye or water surfaces.

The word image is also used in the broader sense of any two-dimensional figure such as a map, a graph, a pie chart, or an abstract painting. In this wider sense, images can also be rendered manually, such as by drawing, painting, carving, rendered automatically by printing or computer graphics technology, or developed by a combination of methods, especially in a pseudo-photograph.

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Image

An image is a rectangular grid of pixels. It has a definite height and a definite width counted in pixels. Each pixel is square and has a fixed size on a given display. However different computer monitors may use different sized pixels. The pixels that constitute an image are ordered as a grid (columns and rows); each pixel consists of numbers representing magnitudes of brightness and color.

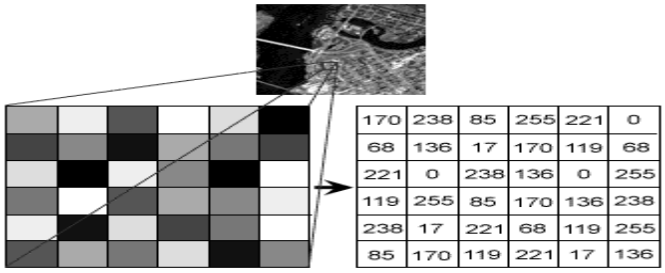

Fig Representation of image in pixel.

Each pixel has a color. The color is a 32-bit integer. The first eight bits determine the redness of the pixel, the next eight bits the greenness, the next eight bits the blueness, and the remaining eight bits the transparency of the pixel.

Fig : Pixel format

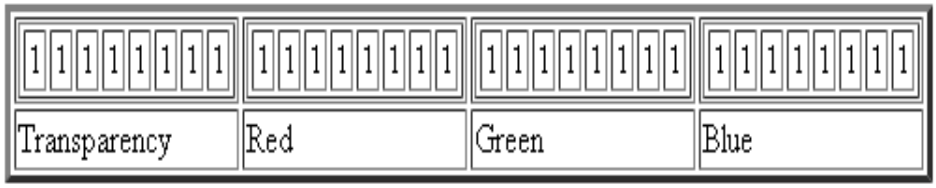

IMAGE RETRIVAL

Image retrieval (lR) is one of the most popular research areas of the image processing. At present, most web-based image search engines rely purely on metadata such as tags, keywords or descriptions which are linked with images, and this may produce a lot of false detection; Besides,

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having humans manually enter keywords for images in a large database can be inefficient and may not capture every keyword that describes the image. Therefore, performances of these systems are not satisfactory. CBIR has now become essential because it can effectively overcome the above problems. The basic objective of CBIR is to extract visual features of images automatically, like color, texture, shape or something more abstract; and compute the similarity degree between images according to similarity measures.

As a result, feature representations and similarity measures are the two key factors which affect the performance of CBIR. CBIR remains to be a difficult problem in both academia and industry which is mainly due to the well-known semantic gap issue that exists between low-level image pixels captured by machines and high-level semantic concepts perceived by human. To fill this gap, Machine learning is one promising technique in the long term [1]. Recent years have witnessed some important advances of new techniques in machine learning. One important breakthrough technique is known as deep learning, which includes a family of machine learning algorithms that attempt to model high-level abstractions in data by employing deep architectures composed of multiple nonlinear transformations [2], [3]. CNNs is one kind of the algorithms, and in this paper, we use CNNs to generate feature representations. Hashing methods are not considered, because this paper focuses on the generalization of the original CNN features, though hashing is helpful. Moreover, SVM is used to learn similarity measures.

EXPERIMENTS AND RESULTS ANALYSIS

Here we had analyzed nearly 6000 images of different types of image database. Where testing and training of content-based images in done at most accuracy for the test u=images and training of dataset gives better results than the existing technique.

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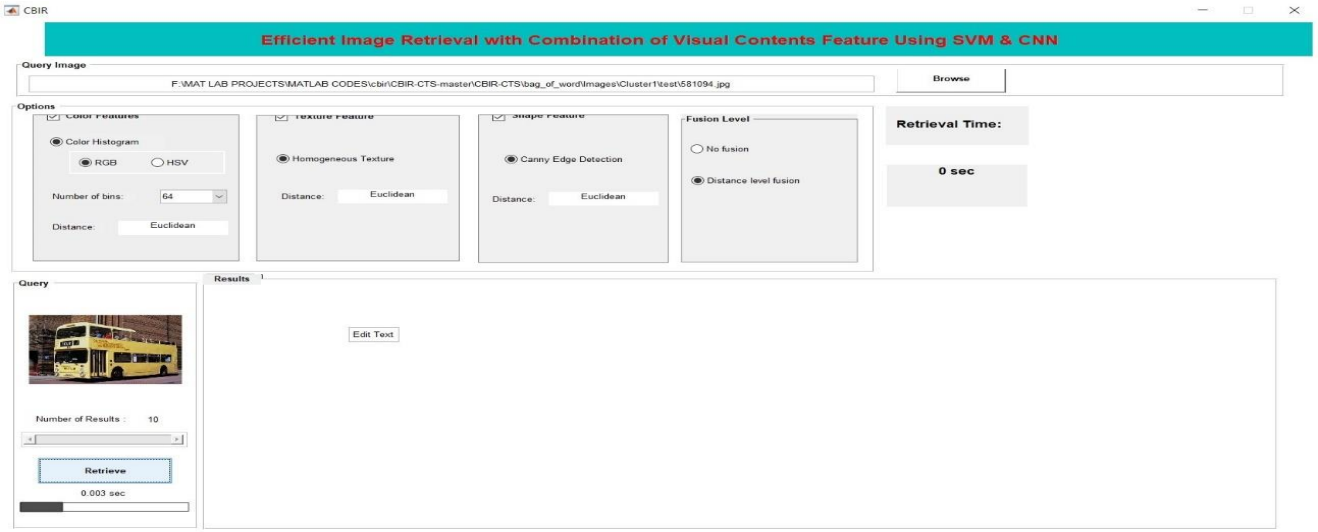
All SVM experiments were carried out in the case of 6000 training samples. The results marked with * are taken directly from the study in our database. As shown we get the same results based on content based images that are similar to the query image. By using deep features in object retrieval tasks performs significantly better than classical features. Besides, the proposed method have succeeded in improving the mAP with SVM. mAP may be related to the following factors.



Architecture of proposed system CBIR using SVM and CNN

CONCLUSION

Applying CNNs to CBIR is a good way to address the long-standing fundamental feature representation problem. This paper proposed a CBIR system based on CNN and SVM, where CNN is used to extract the feature representations and SVM is used to learn the similarity measures. In the training of SVM, generating a validation set helps to tune the parameters. CBIR works well in compressing the deep features in our method by testing, shaping and texture features. We actually have conducted other experiments such as Landmark Image Retrieval, but our method performs poorly. As far as we concerned, the huge gap between the landmark datasets and Imagenet, which is the training dataset of the pre-trained CNN, leads to the poor learning because a linear SVM may not be able to fill the gap. We try to use fusion output to CNN-SVM in our method, but the retrieval processing turns out to be most efficient. The outcomes of the proposed method is better then the previous method.

REFERENCES

[I] R. Datta, D. Joshi, 1. Li, and et aI, "Image retrieval: Ideas, influences, and trends of the new age," Acm Computing Surveys. 2008.

[2] Y. Bengio, A. Courville, and P. Vincent, "Unsupervised feature learning and deep learning: A review and new perspectives," 2012.

[3] L. Deng, "A tutorial survey of architectures, algorithms, and applications for deep learning - erratum," Apsipa Transactions on Signal & Information Processing. vol. 3,2014.

[4] A. S. Razavian, H. Azizpour, 1. Sullivan, and et aI, "Cnn features offthe-shelf: An astounding baseline for recognition," IEEE Conference on Computer Vision and Pattern Recognition Workshops, pp. 512- 519,2014.

[5] 1. Donahue, Y. Jia, O. Vinyals, and et aI, "Decaf: A deep convolutional activation feature for generic visual recognition," Computer Science. vol. 50, pp. 815-830,2013. [6] A. Babenko, A. Slesarev, A. Chigorin, and et aI, "Neural codes for image retrieval," vol. 8689, pp. 584-599,2014.

[7] J. Wan, D. Wang, S. C. H. Hoi, and et aI, "Deep learning for contentbased image retrieval: A comprehensive study," ACM International Conference on Multimedia, pp. 157-166,2014.

[8] K. Simonyan and A. Zisserman, "Very deep convolutional networks for large-scale image recognition," Computer Science. 2014.

[9] A. Krizhevsky, I. Sutskever, and G. E. Hinton, "Imagenet classification with deep convolutional neural networks," Advances in Neural Information Processing Systems. vol. 25, pp. 2649- 2661, 2012.

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ANDROID BASED HOME AUTOMATION SYSTEM USING ARDUINO

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ABSTRACT

The main objective of this project is to develop a home automation system using an Arduino board with Bluetooth being remotely controlled by any Android OS smart phone. As technology is advancing so houses are also getting smarter. Modern houses are gradually shifting from conventional switches to centralized control system, involving remote controlled switches. Presently, conventional wall switches located in different parts of the house makes it difficult for the user to go near them to operate. Even more it becomes more difficult for the elderly or physically handicapped people to do so. Remote controlled home automation system provides a most modern solution with smart phones. In order to achieve this, a Bluetooth module is interfaced to the Arduino board at the receiver end while on the transmitter end, a GUI application on the cell phone sends ON/OFF commands to the receiver where loads are connected. By touching the specified location on the GUI, the loads can be turned ON/OFF remotely through this technology. The loads are operated by Arduino board through optoisolators and thyristors using triacs.

INTRODUCTION

Nowadays, we have remote controls for our television sets and other electronic systems, which have made our lives real easy. Have you ever wondered about home automation which would give the facility of controlling tube lights, fans and other electrical appliances at home using a remote control? Off-course, Yes! But, are the available options cost-effective? If the answer is No, we have found a solution to it. We have come up with a new system called Arduino based home automation using Bluetooth. This system is super-cost effective and can give the user, the ability to control any electronic device without even spending for a remote control. This project helps the user to control all the electronic devices using his/her smartphone. Time is a very valuable thing. Everybody wants to save time as much as they can. New technologies are being introduced to save our time. To save people's time we are introducing Home Automation system using Bluetooth . With the help of this system you can control your home appliances from your mobile phone. You can turn on/off your home appliances within the range of Bluetooth.

DESCRIPTION

ARDUINO UNO Arduino is an open source computer hardware and software company, project, and user community that designs and manufactures single-board microcontrollers and microcontroller kits for building digital devices and interactive objects that can sense and control objects in the physical and digital world. The project's products are distributed as open-source hardware and software, which are licensed under the GNU Lesser General Public License (LGPL) or the GNU General Public License (GPL), permitting the manufacture of Arduino boards and software distribution by anyone. Arduino boards are available commercially in preassembled form, or as do-it-yourself (DIY) kits. Arduino board designs use a variety of microprocessors and controllers. The boards are equipped with sets of digital and analog input/output (I/O) pins that may be interfaced to various expansion boards or Breadboards (shields) and other circuits. The boards feature serial communications interfaces, including Universal Serial Bus (USB) on some models, which are also used for loading programs from personal computers. The microcontrollers are typically programmed using a dialect of features from the programming languages C and C++. In addition to using traditional compiler toolchains, the Arduino project provides an integrated development environment (IDE) based on the Processing language project. The Arduino project started in 2003 as a program for students at the Interaction Design Institute Ivrea in Ivrea, Italy, aiming to provide a low-cost and easy way for novices and professionals to create devices that interact with their environment using sensors and actuators. Common examples of such devices intended for beginner hobbyists include simple robots, thermostats, and motion detectors.

OVERVIEW

HC-05 module is an easy to use Bluetooth SPP (Serial Port Protocol) module,designed for transparent wireless serial connection setup.The HC-05 Bluetooth Module can be used in a Master or Slave configuration, making it a great solution for wireless communication.This serial port bluetooth module is fully qualified Bluetooth V2.0+EDR (Enhanced Data Rate)3Mbps Modulation with complete 2.4GHz radio transceiver and baseband. It uses CSR Bluecore 04- External single chip Rluetooth system with CMOS technology and with AFH (Adaptive Frequency Hopping Feature). Bluetooth Module HC-05 The Bluetooth module HC-05 is a MASTER/SLAVE module.By default the factory setting is SLAVE.The Role of the module (Master or Slave) can be configured only by AT COMMANDS.The slave modules cannot initiate a connection to another Bluetooth device, but can accept connections.Master module can

initiate a connection to other devices.The user can use it simply for a serial port replacement to establish connection between MCU and GPS, PC to your embedded project, etc.

APPLICATIONS

Home Is Where the Smart Is

Evmachine-to-machine communication, and you understand you're not the most tech-savvy consumer, it's impossible that you've missed the abundance of home automation products filling the shelves and ads of every home improvement store. Suddenly an ordinary errand for light bulbs will leave you wondering if your lamp could send you a message alerting you that the light bulb needs to be replaced. Furthermore, if your lamp is talking to you, could your refrigerator and sprinkler system be too? Experts say: Yes, the possibilities are endless. If that's the case, where do you begin? Any day-to-day, repeatable process is automatable with smart home applications.

The greater the control and flexibility of these processes, the more energy and cost savings the resident experiences, which are factors anyone who pays utilities strives to moderate. The smart home revolution is likely to be more of an evolution, with the incorporation of one or two home systems at a time, gradually automating our households through smart mobile devices. However, with these elements of efficiency comes the question of ease of use. Will it bring you enjoyment or exasperation? With so many brands and models already available in an ever growing market, how do you know which is best for you? Lighting Control: Leaving the Dark Ages and Stepping Into the Light Smart lighting allows you to control wall switches, blinds, and lamps, but how intuitive is a lighting control system? It turns out, quite; its capabilities are extensive. You're able to schedule the times lights should turn on and off, decide which specific rooms should be illuminated at certain times, select the level of light which should be emitted, and choose how particular lights react through motion sensitivity, as seen with Belkin's WeMo Switch + Motion, which is both affordable and easy to use with its plug-and-play simplicity.

Security Systems: Knock, Knock… Who's there?

The Internet of Things. While efficiency and conservation are certainly IoT benefits, its potential to have improved control over home security is a primary focus. Smart locks, like Kwikset's Kevo, a Bluetooth enabled electronic deadbolt, and various connected home security systems, such as iSmartAlarm, offer a variety of features including door and window sensors, motion

detectors, video cameras and recording mechanisms. All of which are connected to a mobile device and accessible via the cloud, thus enabling you to access real-time information on the security status of your home. Naturally, there is a great deal of scrutiny regarding the level of trust in controlling your home's security system via a mobile device, but it begs earnest exploration when weighing the potential benefits and peace of mind it provides homeowners.

CONCLUSION

The system as the name indicates, 'Home automation' makes the system more flexible and provides attractive user interface compared to other home automation systems. In this system we integrate mobile devices into home automation systems. A novel architecture for a home automation system is proposed using the relatively new communication technologies. The system consists of mainly three components is a BLUETOOTH module, Arduino microcontroller and relay circuits. WIFI is used as the communication channel between android phone and the Arduino microcontroller. We hide the complexity of the notions involved in the home automation system by including them into a simple, but comprehensive set of related concepts. This simplification is needed to fit as much of the functionality on the limited space offered by a mobile device's display. This paper proposes a low cost, secure, ubiquitously accessible, auto-configurable, remotely controlled solution. The approach discussed in the paper is novel and has achieved the target to control home appliances remotely using the WiFi technology to connects system parts, satisfying user needs and requirements. WiFi technology capable solution has proved to be controlled remotely, provide home security and is costeffective as compared to the previously existing systems. Hence we can conclude that the required goals and objectives of home automation system have been achieved. The system design and architecture were discussed, and prototype presents the basic level of home appliance control and remote monitoring has been implemented. Finally, the proposed system is better from the scalability and flexibility point of view than the commercially available home automation systems.

BIBLOGRAPHY:

- The 8051 Micro controller and Embedded Systems
  - MuhammadAliMazidi
  - JaniceGillispieMazidi
- The8051MicrocontrollerArchitecture,Programming& Applications
  - KennethJ.Ayala
- Fundamentals of Micro processors and Micro computers
  - B. Ram
- Electronic Components
  - D.V.Prasad