

Bank Locker Security System with Password and Intruder Alarm

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Abstract: The main goal of this paper is to design and implement a bank locker security system based using Keypad which can be organized in bank, secured offices and homes. In this system only authentic person can be recovered money from bank locker. We have implemented a bank locker security system technology containing door locking system using PASSWORD which can activate, authenticate, and validate the user and unlock the door in real time for bank locker secure access. The main advantage of using password is more secure than other systems. This system consists of microcontroller, keypad, vibration sensor, and LCD, in this system the keypad reads the password from user and send to the microcontroller, if the password is true then microcontroller send signal to motor driver microcontroller, which will verify the passwords entered by the key board and received from authenticated mobile phone. if these passwords are matched the locker will be opened otherwise it will be remain in locked position, This system is more secure than other systems because two passwords required for verification. This system also creates a log containing check-in and check-out of each user along with basic information of user.

Keywords: *vibration sensor locking system, Keyboard, Microcontroller*

Introduction

In this present age, safety has becomes an essential issue for most of the people especially in the rural and urban areas. Some people will try to cheat or steal the property which may endanger the safety of money in the bank, house, and office. To overcome the security threat, a most of people will install bunch of locks or alarm system. There are many types of alarm systems available in the market which utilizes different types of sensor. The sensor can detect different types of changes occur in the surrounding and the changes will be processed to be given out a alert according to the pre-set value. By the same time this system may not be good for all the time. In this paper we have implemented safety of the money in the bank locker, house, and office by using RFID and which will be more secure than other systems. Radio-frequency identification based access-control system allows only authorized persons to open the bank locker technology. Basically, a system consists of an antenna or coil, a transceiver (with decoder) and a transponder electronically programmed with unique information. There are many different types of systems in the market. These are categorized on the basis of their frequency ranges. Some of the most commonly used kits are low-frequency mid-frequency and high-frequency passive tags are lighter and less expensive than the active Global system for mobile communication is a globally accepted standard for digital cellular communication. is a common European mobile telephone standard for a mobile cellular radio system operating at In the current work, module is used. The module is a Triband solution in a compact plug in module featuring an industry-standard interface. It delivers voice, data and fax in a small form factor with low power consumption in this paper we have designed and implemented a bank locker security system based on in this system only authentic person can be recovered money from bank locker with two password protection method.

Related Works

In this section some related works connected to the monitoring system using GSM services. In [4] has developed a Prepaid Water Meter System for prepaid billing of water consumption through remote monitoring without any human involvement. This system may be fast and accurate billing of water as well as preventing any mishandling of it. However, [5] developed a water meter reading system that suitable for remote places to monitor the water meter reading before any billing process. This could reduce the use of human resource for reading the meter and issuing a bill. There was also a work on monitoring of electrical meter reading using GSM network done by [6]. The system was able of monitoring the meter reading and sent an SMS to the official center for billing purpose. This could reduce the number of estimated reading when the empower person unable to reach the meter.

In [7], this system is used to control home appliance tenuously and offer security when the owner is away from the place. The similar work presented in [8] which designed and developed a smart home application system. The system allows the property owner to be able to monitor and control the residence appliances via a mobile phone set by sending commands in the form of SMS messages and receiving the home appliances status

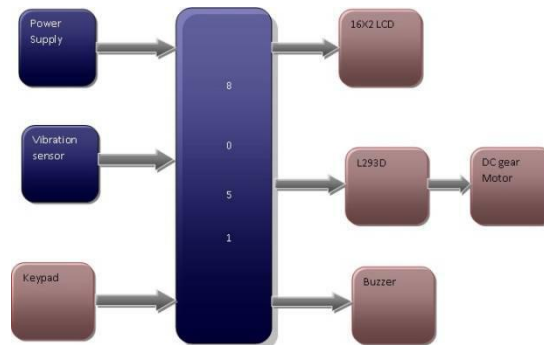
In [9], one more approach using GSM technology to communicate with the remote devices via SMS is remote metering system, in this paper illustrates a technique for remotely reading electricity meter readings using SMS. Both postpaid and prepaid are feasible to implement using this architecture as SMS based data gathering can be done very quickly and efficiently.

In [10] [11], this paper projected a Zigbee-GSM based Monitoring and Remote Control System. In this systems used both Zigbee and GSM for communicating between user and devices. This system allows user to monitor and control devices in the home through a number of controls, including a Zigbee based remote control. Users may remotely monitor and control their home devices using GSM.

In [12], the most important objective of the paper is to design and develop a highly developed vehicle locking system in the real time situation. The design & development of a theft control system for an automobile, which is being used to prevent/control the theft of a vehicle. This system consists of an embedded system and Global System Mobile communication (GSM) technology. This system developed by Pravada P. Wan hade and Prof. S.O. Dahad, the developed system is installed in the vehicle. The mobile is connected to the microcontroller, which is in turn, connected to the engine. Once, the vehicle is being stolen, the information is being used by the vehicle owner for further processing. The information is passed onto the central processing insurance system which is in the form of the SMS, the microcontroller unit reads the SMS and sends it to the Global Positioning System (GPS) module and says to lock it or to stop the engine immediately. The main concept of this paper vehicle is controlled by GSM and GPS. The designed unit is reliable and efficient system for providing security to the vehicles through GSM, GPS and serial communication.

Then the account holder need to enter the password, if the password is valid then microcontroller sends the SMS to account holder mobile number. Then account holder sends the password to the microcontroller through mobile phone using GSM. The microcontroller compares the passwords entered by keyboard and received through mobile phone. If these passwords are correct the microcontroller provides necessary control signal to open the bank locker. This method is simple and more secure than other system.

Block diagram



at pin2 (RX) of the GSM modem. The GSM modem transmits the signal from pin3 (TX) to the microcontroller through MAX232, which is received at pin 10 of IC1. secondary output of 12V, 500 mA. The transformer output is rectified by a full-wave rectifier comprising diodes D1 through D4, filtered by capacitor C1 and regulated by ICs 7812 (IC2) and 7805 (IC3). Capacitor C2 bypasses the ripples present in the regulated supply. LED1 acts as the power indicator and R1 limits the current through LED1. The power supply section is shown in the figure - 1.

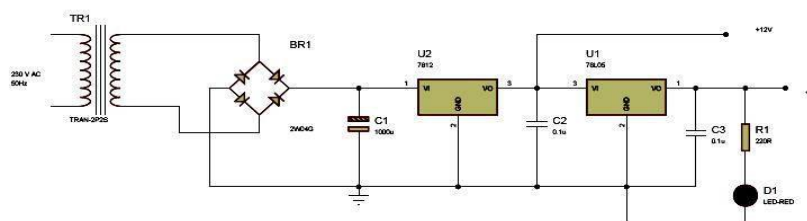


Fig-1: Power supply

Circuit Diagram

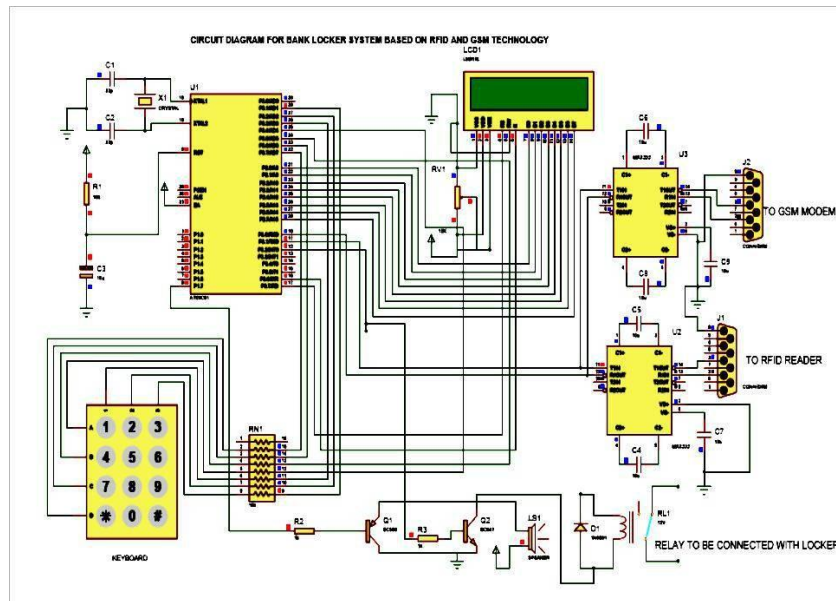


Fig-2: Circuit diagram of Bank locker system

Fig.2 shows the circuit of the Bank locker system based on RFID and GSM technology. The compact circuitry is built around Atmel AT89C52 microcontroller. The AT89C52 is a low-power; high performance CMOS 8-bit microcomputer with 8 kB of Flash programmable and erasable read only memory (PEROM). It has 256 bytes of RAM, 32 input/output (I/O) lines, three 16-bit timers/ counters, a six-vector two-level interrupt architecture, a full-duplex serial port, an on-chip oscillator and clock circuitry. The system clock also plays a significant role in operation of the microcontroller. An 11.0592MHz quartz crystal connected to pins 18 and 19 provides basic clock to the microcontroller. Power-on reset is provided by the combination of electrolytic capacitor C3 and resistor R1. Port pins P2.0 through P2.7 of the microcontroller are connected to data port pins D0 through D7 of the LCD, respectively. Port pins P3.7 and P3.6 of the microcontroller are connected to register-select (RS) and enable (E) pins of the LCD, respectively. Read/write R/W pin of the LCD is grounded to enable for write operation. All the data is sent to the LCD in ASCII format for display. Only the commands are sent in hex form. Register-select (RS) signal is used to distinguish between data (RS=1) and command (RS=0). Preset RV1 is used to control the contrast of the LCD. Resistor 10k limits the current through the backlight of the LCD. Port pins P3.0 (RXD) and P3.1 (TXD) of the microcontroller are used to interface with the RFID reader through Max232(1) and GSM Modem are used to interface through Max232(2). When an allowed person having the tag enters the RF field generated by the RFID reader, RF signal is generated by the RFID reader to transmit energy to the tag and retrieve data from the tag. Then the RFID reader communicates through RXD and TXD pins of the microcontroller for further processing. Thus on identifying the authorized person, the authorized person enters the password through keyboard and send to the microcontroller. If the password is correct then the microcontroller send the SMS to the account holder person, account holder again send the password through SMS to the microcontroller. The microcontroller verifies the password and received password through GSM mobile. If this password is correct, the microcontroller provides high signal to port pin P3.2, transistor Q2 drives into saturation, and relay RL1 energizes to open the bank locker. Simultaneously, the LCD shows “access granted” message and send to and port pin P1.7 drives piezo buzzer PZ1 via transistor T1 for aural indication. If the password is not valid, the LCD shows “access denied” and the bank locker doesn't open.

Software Program Testing

The software program is written in c or assembly language and compiled using keil software. After compiler operation the hex code is generated and stored in the computer. The hex code of the program is burnt into the AT89C51 by using Top win Universal programmer.

A. Hardware Assembling and Testing:

First step, we need to make single side PCB layout of the Bank locker system based on RFID and GSM technology for testing the circuit, proceed as follow

1. After assembling all the components on the PCB, connect TX and RX pins of the GSM modem to pins 13 and 14 of MAX 232 and RFID Reader, respectively and insert a valid SIM in the card holder of the GSM modem.
2. Connect ground pins of the GSM modem and RFID to the ground rail of the circuit.
3. These projects are implemented and tested successfully by us.
4. This system is very useful for bank locker, office, homes to keep the money safely.

Table-1: Comparative study of existing and proposed locker system

S.No	Existing system	Proposed system
1	RFID Technologies used	Rfid and GSM Technologies used
2	One password is referred	Two password are referred
3	May be in Secured due to robbery of RFID and password	More secured due to double password

Conclusions

We have implemented a Bank locker security system using passive RFID and GSM. It is a low cost, low in power conception, compact in size and standalone system. The microcontroller compares the passwords entered by keyboard and received through mobile phone. If these passwords are correct the microcontroller provides necessary control signal to open the bank locker. Alarm will be turn on whenever door is forced to open. Future work of this paper, is planned to a develop security system based on 3G camera for visual identification of the person.

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ENHANCEMENT OF SATELLITE IMAGE USING DUAL TREE COMPLEX WAVELET TRANSFORM

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ABSTRACT

Resolution enhancement (RE) schemes (which are not based on wavelets) suffer from the drawback of losing high frequency contents (which results in blurring). The discrete wavelet-transform-based (DWT) RE scheme generates artifacts (due to a DWT shift-variant property). A wavelet-domain approach based on dual-tree complex wavelet transform (DT-CWT) and nonlocal means (NLM) is proposed for RE of the satellite images. A satellite input image is decomposed by DT-CWT (which is nearly shift invariant) to obtain high-frequency sub bands. The high-frequency sub bands and the low-resolution (LR) input image are interpolated using the Lanczos interpolator. The high frequency sub bands are passed through an NLM filter to cater for the artifacts generated by DT-CWT (despite of its nearly shift invariance). The filtered high-frequency sub bands and the LR input image are combined using inverse DT-CWT to obtain a resolution-enhanced image. Objective and subjective analyses reveal superiority of the proposed technique over the conventional and state-of-the-art RE techniques.

Key Words:

Dual-tree complex wavelet transform (DT-CWT), Lanczos interpolation, resolution enhancement (RE), shift variant.

INTRODUCTION

For many digital image/video processing applications increasing the spatial resolution is highly beneficial. At higher resolution, TV pictures look more natural and pleasing to the eye, computer vision tasks such as object detection and tracking can be performed with higher precision, medical diagnoses can be made with a higher confidence, security cameras can offer better identification, and satellite imagery can be interpreted with higher accuracy. As such, spatial resolution is an influential parameter in many mainstream imaging applications, and resolution enhancement task naturally arises as a means of increasing the effectiveness of any imaging system used in the mentioned applications. In this thesis, we concentrate on two enhancement problems of practical importance, namely, low-complexity resolution enhancement for customer grade flat panel televisions, and resolution enhancement of noisy high-dimensional hyper spectral imagery. For TV resolution enhancement our main concern is keeping computational complexity at a minimum. The hardware limitations of average customer grade televisions effectively rule out a multiform approach. Hence, we take a low-complexity single-frame approach based on exploiting natural image characteristics. Flat panel display technology is probably one of the fastest growing video display technologies with advancements taking place in all areas. Compared to the conventional cathode ray tube (CRT) displays, flat panel displays offer same screen size in much thinner forms, consume less energy, and virtually eliminate the infamous flicker problem 1 of the 1See Appendix

A for a description of the flicker problem.

- Resolution enhancement schemes suffer from the drawback of losing high frequency contents .
- The discrete wavelet- transform-based RE scheme generates artifacts
- Resolution is the limiting factor for the utilization of remote sensing data.
- Therefore, spectral, as well as spatial, resolution enhancement (RE) is desirable.
- Interpolation has been widely used for RE. Commonly used interpolation techniques are based on nearest neighbors (include nearest neighbor, bilinear, bicubic, and Lanczos).
- The Lanczos interpolation (windowed form of a sinc filter) is superior than its counterparts (including nearest neighbor, bilinear, and bicubic) due to increased ability to detect edges and linear features.
- It also offers the best compromise in terms of reduction of aliasing, sharpness, and ringing .

EXISTING SYSTEM

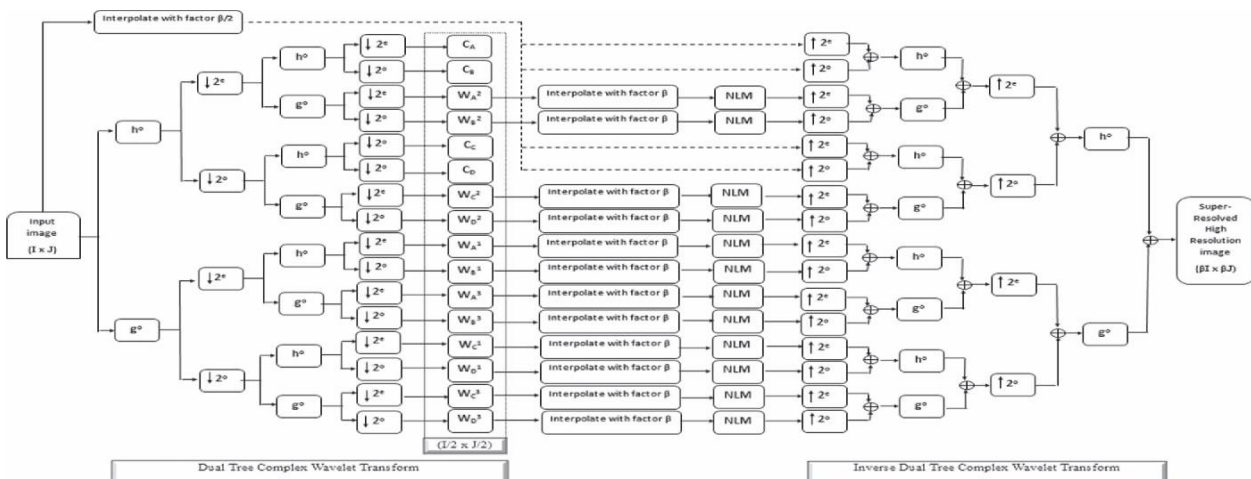
Interpolation has been widely used for RE . Commonly used interpolation techniques are based on nearest neighbors .The Lanczos interpolation is superior to its counterparts due to increased ability to detect edges and linear features. It also offers the best compromise in terms of reduction of aliasing, sharpness, and ringing Methods based on vector-valued image regularization with partial differential equations and inpainting and zooming using sparse representations are now state of the art in the field .

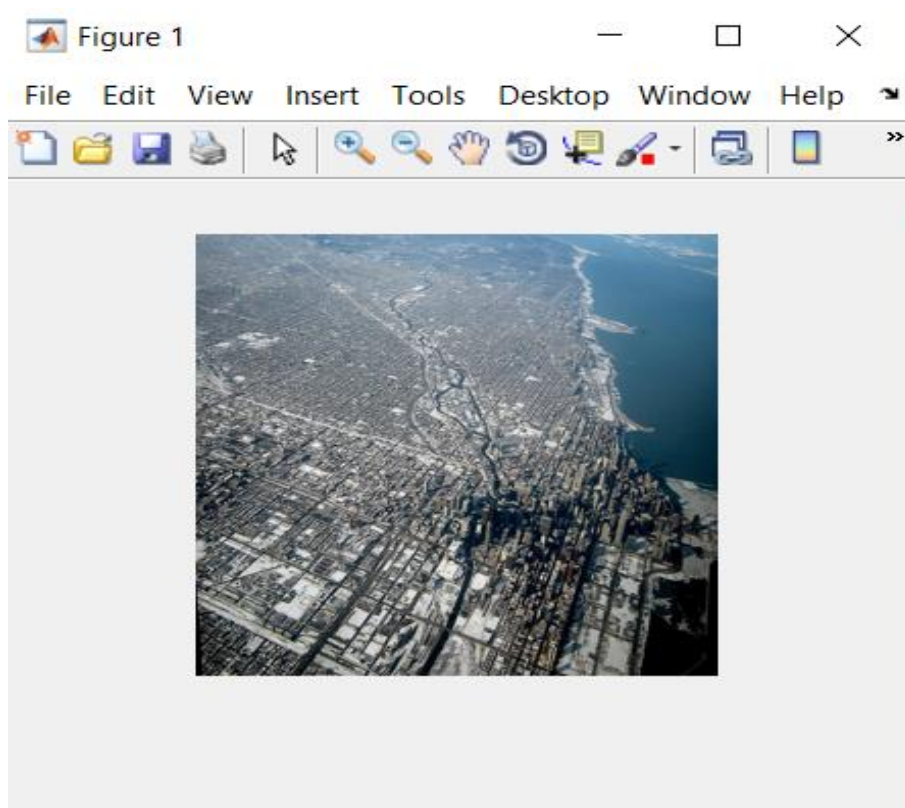
DISADVANTAGE

- RE schemes suffer from the drawback of losing high-frequency contents which results in blurring.
- Quality of image will be reduced.
- High loss of data
- Requires more time to evaluate the performance of the filtered output

PROPOSED SYSTEM

A DT-CWT-based nonlocal-means-based RE technique is proposed, using the DT-CWT, Lanczos interpolation, and NLM. Note that DT-CWT is nearly shift invariant and directional selective. Moreover, DT-CWT preserved the usual properties of perfect reconstruction with well-balanced frequency responses . Consequentially, DT-CWT gives promising results after the modification of the wavelet coefficients and provides less artifacts, as compared with traditional DWT.





ADVANTAGES

- Reduces blurring effect by using DT-CWT technique.
- It improves the quality of an image by removing residuals.

CONCLUSION

An RE technique based on DT-CWT and an NLM filter has been proposed. The technique decomposes the LR input image using DT-CWT. Wavelet coefficients and the LR input image were interpolated using the Lanczos interpolator. DT-CWT is used since it is nearly shift invariant and generates less artifacts, as compared with DWT. Finally the enhanced filtered output image is obtained with high quality resolution image.

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A REVIEW ON HIGH SPEED 32-BIT VEDIC MULTIPLIER DESIGN AND IMPLEMENTATION

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ABSTRACT

The proposed research work indicates the changed variant of parallel Vedic multiplier utilizing Vedic sutras of old Vedic science. It gives change in for starters carried out Vedic multiplier. The changed paired Vedic multiplier is ideal has shown improvement in the particulars of the time deferral to greatest conceivable degree and furthermore gadget use. The proposed procedure was planned and executed in Verilog HDL though LUT were fortify and time delay is improved. For HDL simulation, modalism instrument is utilized and for circuit synthesis, Xilinx is utilized. The simulation has been accomplished for 4-bit, 8-bit, 16-bit, 32-bit increase activity. Just for 32-bit parallel Vedic multiplier strategy the simulation results are shown. This changed increase method is reached out for bigger sizes. The results of this augmentation procedure are contrasted and existing Vedic multiplier strategies.

Index Terms:

Vedic multiplier, Ripple carry adder, Verilog HDL, Simulation, synthesis.

INTRODUCTION

CMOS technology dominates VLSI and other logic families. But this technology has some drawbacks which have been solved. For an instance, the process technology has reduced the size from 180nm in 1999 to 60nm in 2008. Now it is reduced to 45nm. Several attempts being made to reduce it 32nm. However, die area shrunk during 2008 now is increasing due to the greater number of transistors and its features. Vedic multiplies with different architecture is designed using carry save adder and ripple carry adder. Performances are compared and their merits and demerits are identified with respect to speed and area focused in Adiabatic logic is utilized to minimize power consumption of Vedic multiplier and its performance is estimated by comparing it with traditional MOS design Vedic multiplier with adiabatic logic consumes less power than Vedic multiplier without adiabatic logic analysed in. FinFET implies Fin Field Transistor. The power and zone productive plan of full adder with 6 transistors utilizing proposed 2 transistors XOR gate has been displayed. The pass transistor is used to decrease the transistor count for any implementation logics utilizing privacy input to drive gate terminals, source and drain terminals. Multiplies is an important component in digital signal processing



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(DSP) and communication systems. It is utilized in signal and image processing applications including convolution, Fast Fourier Transform (FFT) and correlation. Therefore, it is necessary to develop a multiplier with power efficient and speed to reduce the cost of the systems. It is based on 16 algorithms. The main advantage is the use of FinFET which provide numerous profits and advantages over the bulk CMOS.

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. We discuss a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Triyakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. In this paper, after a gentle introduction of this Sutra, it is applied to the binary number system to make it useful in the digital hardware. The hardware architecture of the Vedic multiplier is presented and is shown to be very similar to that of the popular array multiplier. It is also equally likely that many such similar technical applications might come up from the storehouse of knowledge, Veda, if investigated properly [1-3].

In the present age of digital communication various audio visual or any other perception signals are sampled on time [i.e. axis] and are quantized on amplitude [y- axis], to produce discrete version of the continuous signal .This results in the corresponding information being contained in a series of binary (0 & 1) sequence. Hence any processing or transformation of original signal boils down to suitable discrete mathematical operation applied to binary sequences [5-6]. Different algorithms exist to accomplish each of these tasks. The task themselves may include basic arithmetic operations like addition, subtraction, multiplication, division, matrix, squaring, exponential operations etc. While implementing these algorithms on digital computer, the prevalent VAN-NEUMAN architecture uses registers operations like shift, move, Compliment, add etc. to accomplish these basic arithmetic tasks. The actual CPU implementation of these operations is through suitable amalgamation of algorithm and implementing architecture. Though there are many algorithms for the same task only VAN-NEUMAN architectural implementation of classical method is found to be used in present day digital computers. The Vedic mathematical methods suggested by Shankaracharya Sri. Bharti Krishna Tirtha through his book offer efficient alternatives.



INTRODUCTION TO PROJECT-

The term 'Veda' means storehouse of knowledge. Vedic Mathematics is an ancient form of mathematics reconstructed from ancient Indian scriptures referred to as Vedas. It is based on 16 sutras which transact different branches of mathematics like algebra, geometry, arithmetic. Urdhva Tiryagbhyam is the most generalized sutra for implementation of Vedic Multiplier designs because with increase in number of bits both area and delay increase slowly. The beauty of Vedic Multiplier lies in the fact that they can be used to solve cumbersome mathematical operations orally thereby improving speed. Fig.1.1 shows multiplication of 23 and 52 using Urdhva Tiryagbhyam. Multipliers being the key components of Arithmetic and logic units, Digital signal processing blocks and Multiplier and accumulate units, determine the performance and throughput of the applications. Vedic Multiplier has become highly popular as a faster method for computation and analysis. They have found immense use in applications of image processing to save time and area. Image processing is the application of certain operations on images such as image sharpening, pattern recognition, edge detection etc, to extract some useful information from them or to enhance a particular feature in it. Hence it is essential in fields of mapping, holography, x-ray imaging, medical image processing and robotics. Similarly Digital Signal Processing is another area where high speed and low area Vedic Multipliers, are replacing commonly used conventional multipliers.

LITERATURE SURVEY

Multipliers play vital and important role in many of Digital Signal Processing (DSP) and various different applications. Multiplication is mathematical operation in which the number is repeatedly added to itself for the specified number of times. Multipliers take more time and area than any other arithmetic operations. Digital Signal Processing (DSP) applications uses Multipliers in performing various operations in convolution of signals, filters, performing (FFT) Fast Fourier Transform and in microprocessors Arithmetic & Logic Unit (ALU) [1-13].

Multiplication of floating point numbers is greatly significant in many DSP applications Urdhva Tiryagbhyam sutra of Vedic mathematics is used for the design and implementation of single precision floating point multiplier using Verilog. This design implements floating point multiplication with sign bit and exponent calculations.

The results show different parameters in Xilinx ISE 14.7. Full adders are designed for a 16-bit vedic multiplier to decrease number of slices and delay. The results obtained are compared and it is found that the reformed full adders have less delay. The design is implemented using four adders of



different techniques such as full adder using two half adders and an OR gate. Second modified full adder is designed by using XOR gate and 2:1 multiplexer, third modified full adder by using two 4:1 multiplexer and fourth modified full adder using a combination of XOR gate, XNOR gate and a 2:1 multiplexer. After comparing the results, they concluded that the third modified full adder has better performance. Gate diffusion input (GDI) is a method used for describing the structure of low-power digital combinatorial circuit. The GDI technique is implemented using two transistors for a deep range of complex logic design. A high speed 32-bit vedic multiplier is designed.

For addition of partial products in a 32-bit vedic multiplier Kogge stone adder and a ripple carry adder is used. Two multipliers are implemented using these two methods and results are compared with these two multipliers. In 8-bit multiplier which is implemented using Urdhva Tiryagbhyam sutra, the partial product addition is realized using carry skip technique. A digital processor requires a multiplier as it is a basic block in the processor. A 32-bit vedic multiplier is proposed using one carry save adder. The input of multiplier is arranged in two 16-bit numbers to apply it stepwise using Urdhva Tiryagbhyam sutra and the partial product is added using one carry save adder thus reducing the hardware blocks in the circuit. The processors are integrated into one chip as demand of complex processors is increased. But the load on the processor is not reduced. To reduce this load, the main processor is equipped with co-processors.

Design of a hybrid FIR filters using vedic multipliers and fast adders is today's need in many DSP processors. FIR filters play a significant role in the field of digital signal processors to eliminate noise suppression in electro cardio graph, imaging devices and the signal stored in analog media. So filter evaluation is accomplished to reduce the noise level. Multipliers and adders play a vital role in determining the performance of FIR filter. They have proposed modified Annuprya vedic multiplier methods with Kogge Stone fast adder for implementation in the direct form FIR filter. Multipliers play a major role in today's digital signal processing and various other applications. Both signed and unsigned multiplications are required in many computing applications.

EXISTING SYSTEM

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Fig. 3. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier [2]. Hence it is concluded that multiplication of 2-bit binary numbers by Vedic method does not made significant effect in improvement of the multiplier's efficiency. Very precisely we can state that the



total delay is only 2-half adder delays, after final bit products are generated, which is very similar to Array multiplier. So we switch over to the implementation of 4x4 bit Vedic multiplier which uses the 2x2 bit multiplier as a basic building block. The same method can be extended for input bits 4 & 8. But for higher no. of bits in input, little modification is required.

A multiplier of 2 bit is used to calculate intermediate stage results, and the output is 4 bits. (A3A2)(B3B2) using 2 bit multiplier generates result: S33S32S31S30 (A3A2)(B1B0) using 2 bit multiplier generates result: S23S22S21S20 (A1A0)(B3B2) using 2 bit multiplier generates result: S13S12S11S10 (A1A0)(B1B0) using 2 bit multiplier generates result: S03S02S01S00.

PROPOSED VEDIC MULTIPLIER

An Application-Explicit Coordinated Circuit (ASIC) is a fused circuit (IC) revamp for a particular use, rather than proposed for all around helpful use. As feature sizes have contracted and setup mechanical assemblies improved consistently, the most outrageous multifaceted design (and thusly handiness) possible in an ASIC has created from 5,000 ways to in excess of 100 million. Present day ASICs much of the time join entire 32-bit processors, memory squares including ROM, Smash, EEPROM, Streak and other huge construction squares. Such an ASIC is much of the time named a SOC (system on-a-chip). Fashioners of modernized ASICs use a gear portrayal language (HDL, for instance, Verilog or VHDL, to depict the convenience of ASICs. Field-programmable entryway groups (FPGA) are the state of the art advancement for structure a breadboard or model from standard parts; programmable reasoning squares and programmable interconnects license the same FPGA to be used in a wide scope of employments. For smaller plans or conceivably lower creation volumes, FPGAs may be more monetarily keen than an ASIC design even in progress.

SIMULATION RESULTS AND DESCRIPTION

The proposed work uses Modelsim for Verilog HDL simulation and XILINX ISE is used for performing synthesis. The simulations is made for up to 32 bit operations.



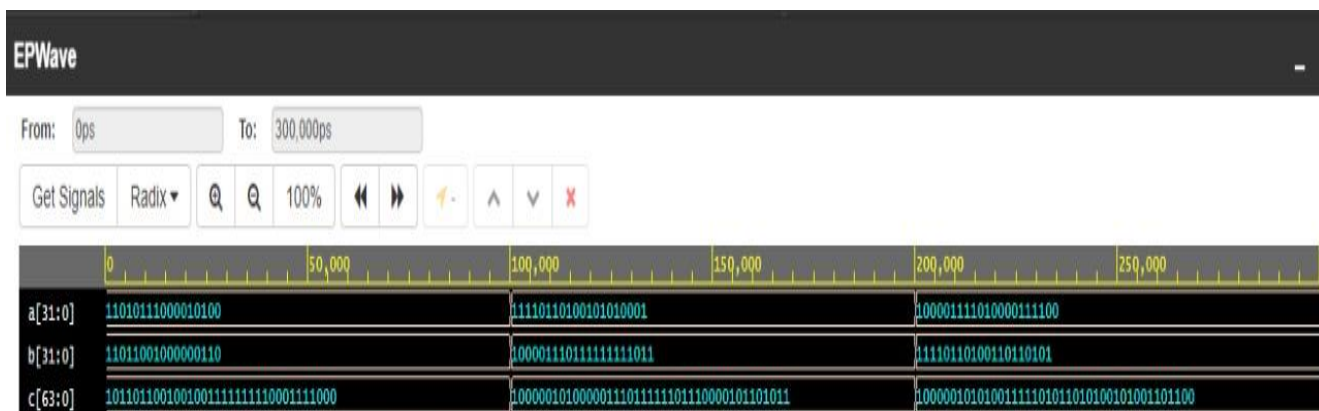
S.No	Bit Size	Basic design units
1	2x2	Four AND gates, Two HAs
2	4x4	Four 2x2 multipliers , CSA for 4-bit addition, OR gate, 2-bit adder
3	8x8	Four 4x4 multipliers, CSA for 8-bit addition, OR gate, 4-bit adder
4	16x16	Four 8x8 multipliers, CSA for 16-bit addition, OR gate, 8-bit adder
5	32x32	Four 16x16 multipliers, CSA for 32-bit addition, OR gate, 16-bit adder

Requirements for modified Vedic multiplier

```

19 // Dependencies:
Log Share
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4837 kB (elbread=447 elab2=4255 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: input_a: 110100,input_b: 111110,output: 12233211000
# KERNEL: input_a: 1010001,input_b: 1110011,output: 1121112220011
# KERNEL: input_a: 1111100,input_b: 1010101,output: 1122323221100
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./wave.vcd
[2021-09-05 09:31:28 EDT] Opening EPWave...
Done

```



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

The waveforms of simulation for Vedic multiplication of 4 bit are shown in the Table 7.1. The modified 4-bit, 32-bit Vedic multiplier the waveforms are displayed in the fig. 7.1, and fig. 7.2. As shown in Table 7.1, the Table I below shows the values of Delay and Area of Vedic Multiplier. The Table II shows the values of Time Delay and Area of Modified Vedic Multiplier.



CONCLUSION

This paper has introduced a deliberate strategy for twofold multiplier [1] circuits which depends on Vedic mathematics. With regards to the terms of time defer then the proposed framework is more effective than existing strategies. Extension for a higher bit size should be possible with assistance of proposed method. Also, adders of various models [5] can be utilized in the CSA Carry Save Adder configuration utilized in the proposed changed Vedic multiplier. Among numerous methods adjusted design is utilized to speed up the augmentation. In this method climb in region happened it is a disadvantage. A consciousness of Vedic mathematics can be viably expanded in case it is remembered for designing training.

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KIDNEY STONES DETECTION USING FUZZY C AND K MEANS CLUSTERING TECHNIQUES : A COMPARISION

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ABSTRACT:

Now a days Medical images are too fuzzy for many discrete boundaries. This thesis describes a fuzzy rule based seed point optimization technique in Fuzzy C-Means clustering technique with an application in segmentation process. The most important information about the concept helps to extend the cluster and able to identify the target seed point smoothly for the detection of renal calculi often called as a kidney stones. This method makes the whole concept an innovative one where Kidney is a source organ for urology disorder which can be protected by efficient kidney stone detection technique in CT images. Proposed method of clustering reduces the number of iterations for elaborating the region of interest in allowed images. This approach gifted to give a more accurate solution for CT images and it enhances the image retrieval as compared to classical clustering approaches. The experimental results justify the effectiveness of proposed approach by reducing the computational time without effecting the segmentation quality in an efficient way.

Keywords:

K-Means clustering, Fuzzy C-Mean, Computed tomography images, Computer Aided Diagnostic system.

INTRODUCTION

Renal calculus, more commonly known as kidney stone formation, is characterized by the formation of crystals in the urine caused by substance concentration or genetic susceptibility. All persons are susceptible to kidney stones, even infants, and yet, the majority of kidney stone cases remain undetected except in cases where extreme abdominal pain is exhibited or abnormal urine color is observed. In addition, people with kidney stones exhibit common signs such as fever, pain and nausea that are easily associated to other conditions. Kidney stone detection is important particularly in its early stages to facilitate intervention or to receive proper medical treatment. The presence or the recurring presence of kidney stone decreases kidney functions and dilation of the kidney. It also has implications on the degrees of chronic kidney disease (CKD) or chronic renal failure (CRF) for people who have not been previously diagnosed with this condition. However, because of its asymptomatic nature, it is commonly diagnosed among patients who undergo medical examination for other diseases such as cardiovascular diseases (CVD), diabetes, and other medical conditions predispose to the urogenital apparatus [1]-[3]. Today, computer-assisted tools such as Manuscript received February 26, 2015; revised June 5, 2015. ultrasound imaging, computed tomography (CT), and Xrays that use intravenous pyelogram (IVP) provide the most accurate diagnostic tools for kidney stone screening and diagnosis. CT scans, which provide threedimensional views of the organ or region of interest is the most sought after kidney stone

screening tool in hospitals. Its convenience and efficiency in kidney stone detection (including its pathology) for both asymptomatic and symptomatic patients make advances in CT technology extremely important for physicians and patients alike [4], [5]. Software programming, which has found current and potential applications in technological advancements in the field of medicine, recognizes the need to contribute to CT screening development particularly in enhancing diagnosis of the kidney-urine-belly (KUB) region for kidney stone detection. This study developed a semiautomatic kidney screening program that integrated digital image processing and image analysis techniques in KUB CT images. Specifically, the study (1) developed a method for defining the boundary of regions of interest in a digital KUB CT scan; (2) developed a method for segmenting the region and object of interest in a digital KUB CT scan; and, (3) developed a method for detecting the object of interest (kidney stones) including its size and location in a digital KUB CT scan images. Fig. 1 shows the cross-section of abdomen.

Medical imaging is a field that has experienced significant advances due to new computer technologies. Digital systems have become an integral part of CT, MRI, PET, SPECT, and Ultrasound imaging and even traditionally non-digital techniques (e.g. film X-rays) are gradually evolving into computerized imaging. However, digital imaging requires storing, communicating and manipulating large amounts of digital data. Studies have shown that the radiology department of a large hospital can produce more than 20 terabits of image data per year.

The amount of digital radiologic data generated every year in the USA alone is on the order of petabytes (10^{15}) and is increasing rapidly. This stretches the capabilities of digital storage systems, and imposes exceedingly high requirements on the bandwidth of communication networks.

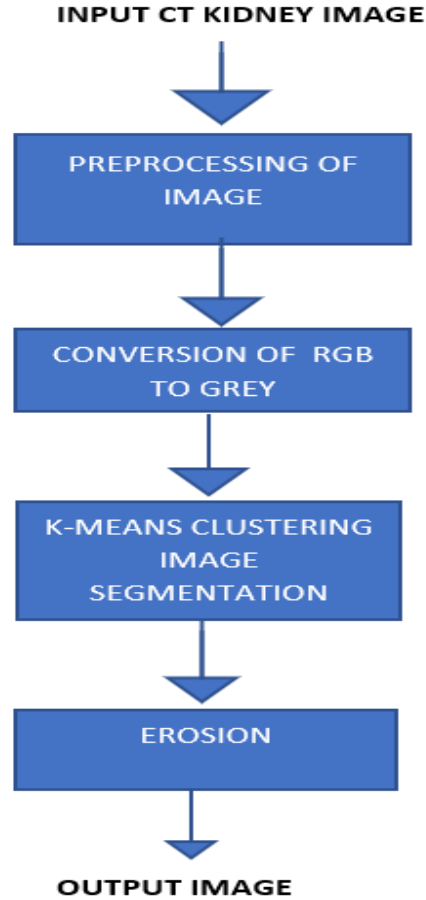
IMAGE COMPRESSION

The objective of image compression is to reduce irrelevance and redundancy of the image data in order to be able to store or transmit data in an efficient form. Digital image compression can address these problems by reducing the data storage and transmission requirements. Many compression methods have been developed and have been evaluated for the medical environment. These compression methods usually reduce the size of the data 2-3 times with no information loss, and more than 10 times with some information loss. Despite the higher compression ratios of lossy compression methods, their use in medical imaging is limited because of concerns on losing image details. Even when the compression is visually lossless, an unsuccessful diagnosis from an image that has lost some information may lead to legal implications. Another reason for avoiding lossy compression is the development of computer aided diagnosis techniques. Computerized analysis of an image can use even the smallest details (e.g., very smooth variations in pixel intensities) which are often invisible to the eye. Compression methods should not lose any of these potentially important image details.

For this reason, in medical imaging lossless compression is more important than lossy compression. In general, lossless compression can be achieved by taking advantage of data redundancies. Existing methods can efficiently reduce data redundancies in individual images.

PROPOSEDMETHOD

BLOCK DIAGRAM



K MEANS AND FCM COMPARISION

Fuzzy C-means Clustering(FCM), is also known as Fuzzy ISODATA, is an clustering technique which is separated from hard k-means that employs hard partitioning. The FCM employs fuzzy partitioning such that a data point can belong to all groups with different membership grades between 0 and 1.

FCM is an iterative algorithm. The aim of FCM is to find cluster centers (centroids) that minimize a dissimilarity function.

To accommodate the introduction of fuzzy partitioning, the membership matrix(U) is randomly initialized according to Equation 3.1

$$\sum_{i=1}^c u_{ij} = 1, \forall j = 1, \dots, n \quad (3.1)$$

The dissimilarity function which is used in FCM is given Equation 3.2

$$J(U, c_1, c_2, \dots, c_c) = \sum_{i=1}^c J_i = \sum_{i=1}^c \sum_{j=1}^n u_{ij}^m d_{ij}^2 \quad (3.2)$$

u_{ij} is between 0 and 1;

c_i is the centroid of cluster i ;

d_{ij} is the Euclidian distance between i_{th} centroid(c_i) and j_{th} data point;

$m \in [1, \infty]$ is a weighting exponent.

To reach a minimum of dissimilarity function there are two conditions. These are given in Equation 3.3 and Equation 3.4.

$$c_i = \frac{\sum_{j=1}^n u_{ij}^m x_j}{\sum_{j=1}^n u_{ij}^m} \quad (3.3)$$

$$u_{ij} = \frac{1}{\sum_{k=1}^c \left(\frac{d_{ij}}{d_{kj}} \right)^{2/(m-1)}} \quad (3.4)$$

Detailed algorithm of fuzzy c-means proposed by Bezdek in 1973[5]. This algorithm determines the following steps [4].

Step 1. Randomly initialize the membership matrix (U) that has constraints in Equation 3.1.

Step 2. Calculate centroids(c_i) by using Equation 3.3.

Step 3. Compute dissimilarity between centroids and data points using equation 3.2. Stop if its improvement over previous iteration is below a threshold.

Step 4. Compute a new U using Equation 3.4. Go to Step 2.

By iteratively updating the cluster centers and the membership grades for each data point, FCM iteratively moves the cluster centers to the "right" location within a data set.

FCM does not ensure that it converges to an optimal solution. Because of cluster centers (centroids) are initialize using U that randomly initialized.(Equation 3.3).

Performance depends on initial centroids. For a robust approach there are two ways which is described below.

1-) Using an algorithm to determine all of the centroids. (for example: arithmetic means of all data points)

2-) Run FCM several times each starting with different initial centroids.

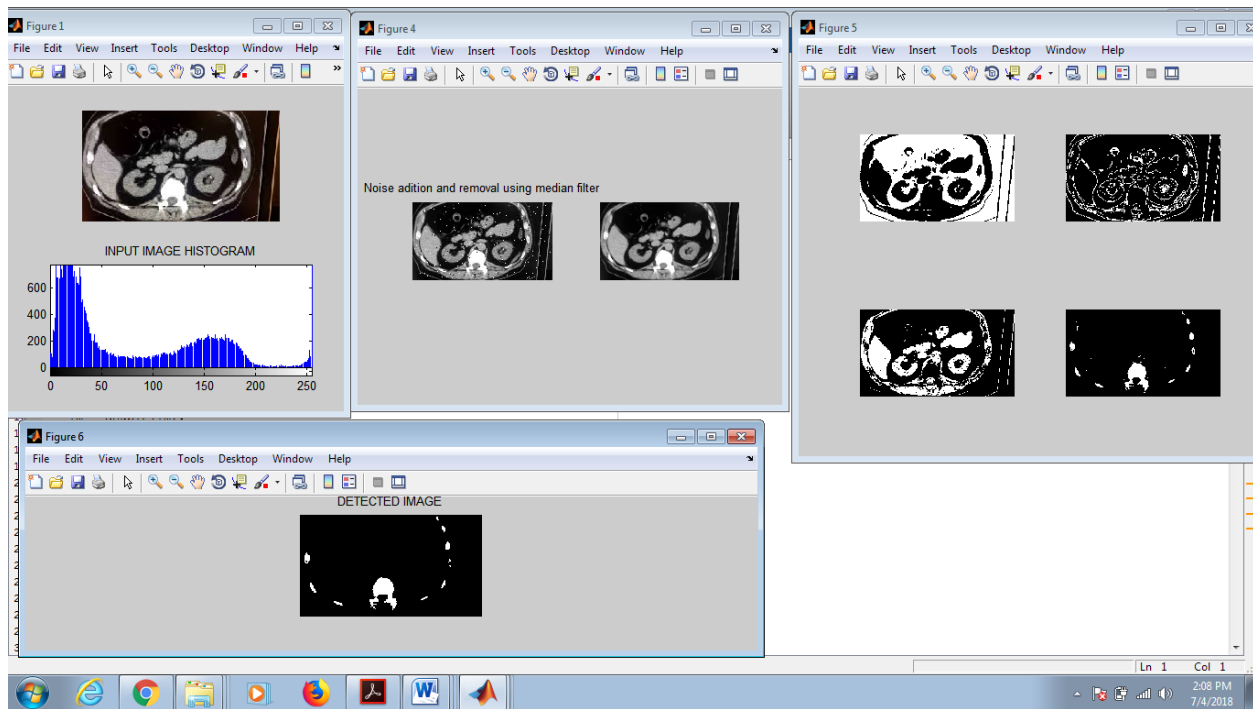
We preferred the first one and obtained the better performance on thyroid gland data.

METHODOLOGY

The digitized transverse abdomen CT scan images were taken with Toshiba Aquilion 16 Slice CT scanner, and obtained from the Imam Reza Hospital in Iran (kums.ac.ir) through their Picture Archiving and Communication System (PACS). KUB CT scans from 39 patients with symptomatic and asymptomatic kidney stone cases in 2014 were provided by the Imam Reza Hospital as subjects for the program prototype application. Each patient has 40 to 48 slices; of these, 10 patients were diagnosed without kidney stones, while the remaining 29 patients were diagnosed with variable kidney stone conditions through their CT scans by the hospital. This is to establish the degree of accuracy and efficiency of the program in distinguishing kidney stone cases which may be authenticated by a specialist. The program design was grounded on the application of image processing techniques and geometry principles. Image processing techniques applied in the program include Contrast Adjustment (Gamma Adjustment) [6], Segmentation [7]-[10], Binarization (Thresholding) [7], [11], [12], morphological

operation [13]-[15], localization [14], Boolean operation [7], [11] and connected component [14], [15], while geometry principles and axioms were used to compute for distances between pixel points and center of mass [16]. These were used integratively in the program to develop six levels of image analyses (localization, contrast adjustment, segmentation, combining [17], connected component labeling [18], and restriction and object detection [19] to enhance kidney stone detection. The following procedures were undertaken: Using the KUB CT scans provided by the Imam Reza Hospital, the program analyzed slices from each patient where the kidney, the region of interest, is only visible. Since not all slices provide a clear view of the kidney, reading of slices begin at Slice 1, however analysis is read and merged where the kidney is visible such as shown in.

RESULT ANALYSIS



CONCLUSIONS

Image analysis prototype was developed to provide technical support in enhanced kidney stone detection. Its function to pinpoint the kidney area as region of interest, and kidney stones as objects of interests provide focused investigation for medical specialists using image processing methods. Here the program's capacity to organize by sequence multiple slices and combine these based on discernible images of the kidney allows the physician to evaluate an aggregate image from various images that the CT machine took for each patient. This provides cost effective and timely delivery of diagnosis for both physician and patients. The ability to detect and mark kidney stones and to identify stone size and location based on pixel values provide more efficient analysis of cases. It has demonstrated potential usefulness in kidney stone diagnosis and screening, however, the program is only a tool and the opinion of a qualified medical professional is required to validate its output.

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RF BASED HOME AUTOMATION USING ARDUINO

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Abstract:

The main object of this project is to develop a home automation system with a two button key fob transmitter by using RF (Radio Frequency) technology. Nowadays, houses are gradually shifting from normal switches to centralized control system, involving a remote control transmitter. This technology is not only easy to use but also helps to prevent miss uses of energy. Remote control (key fob) transmitter is small and very light weight, which will work from a decent distance. In order to achieve this, a RF remote (Keyfob) is interfaced to the microcontroller on transmitter side which sends ON/OFF commands to the receiver where loads are connected. By operating the specified remote switch on the transmitter, the loads can be turned ON/OFF remotely through wireless technology. Arduino IDE software has been used to compile some programs related to the microcontroller ATmega328. (Arduino pro-mini)

Introduction:

An embedded system is a system which is going to do a predefined specified task is the embedded system and is even defined as combination of both software and hardware. A general-purpose definition of embedded systems is that they are devices used to control, monitor or assist the operation of equipment, machinery or plant. "Embedded" reflects the fact that they are an integral part of the system. At the other extreme a general-purpose computer may be used to control the operation of a large complex processing plant, and its presence will be obvious.

All embedded systems are including computers or microprocessors. Some of these computers are however very simple systems as compared with a personal computer.

The very simplest embedded systems are capable of performing only a single function or set of functions to meet a single predetermined purpose. In more complex systems an application program that enables the embedded system to be used for a particular purpose in a specific application determines the functioning of the embedded system. The ability to have programs means that the same embedded system can be used for a variety of different purposes. In some

cases a microprocessor may be designed in such a way that application software for a particular purpose can be added to the basic software in a second process, after which it is not possible to make further changes. The applications software on such processors is sometimes referred to as firmware.

Home automation is a step toward what is referred to as the "Internet of Things," in which everything has an assigned IP address, and can be monitored and accessed remotely. Home Automation is also to be known as "Domotics" or "Domotica" as referred in [1]. It can be considered as extension of building automaton towards residential areas which involves handling or controlling of HVAC systems, security, or various electrical appliances. Conventional systems follow standard structure where switches or sensors are connected to a gateway. A user interface is used to handle the entire system for remote monitoring and can be interacted with any web interface or a static computer machine. Few infrastructure standards of a smart home system are pretty much distributed.

Background

As mentioned in [2], Home automation system involves various software and hardware components being intertwined to interconnect different electrical devices. Using buttons present on the user interface, user from any remote location, can manipulate or regulate HVAC system, switching on/off lights or other appliances timely to save energy. Entire system is laid on a wireless network with TCP/IP connections between the interfaces. The use of IP and MAC addresses eases out the identification of any device under consideration. The use of microcontrollers, sensors and actuators help the system to complete its functionality and work efficiently, thus saving electricity and hence money. All put in together working of 3 components in an orderly manner helps user to save his/her valuable time.

Proposed System

The proposed system is a Home automation system using internet as a medium to transfer user response for controlling devices. It too consists of two modules – User Communication module and Hardware interface module. The software module transmits the response given by the user via Internet/Server to the Arduino. The Arduino relays a corresponding signal and sends to the meant device. The most important part of the system is

a Wireless Ethernet module that is connected to a router. The Ethernet module is also connected to the Arduino. The router after receiving the data sends the signal to the appropriate device using port forwarding. The router generates a Static IP address to make a successful communication with the devices. The Arduino is connected to a Gas sensor and an IR sensor. The System can be accessed from the web browser remotely from any mobile device connected to the Internet. The proposed Home automation System can control the following appliances- Lights On/Off, Air conditioner, Computer On/Off and monitor Gas Leakage at home and motion detection which can activate alarm or adjust temperature of the room accordingly.

The Gas sensor connected to the Arduino senses for the LPG (Butane and Iso-Butane) gas and if detected the Arduino is programmed to send a SMS to the user's Cell phone immediately informing the user of the leakage as in [4]. On the other hand, The IR receiver is used for the Air conditioner. The user sends a signal from the web browser which is further relayed by the router to the Arduino (Web Server) and the Arduino in turn sends the IR response of the particular signal to the Air Conditioner. The IR response depends on the make of the A/C which is programmed in the Arduino as in [5]. In order for operating (switching on/off) computer machine use of WOL (Wake on LAN) technology is used mentioned in [6]. The SMPS has some current being passed through it which can trigger the circuit to be completed and hence switching on the computer system.

The System consists of three modules:

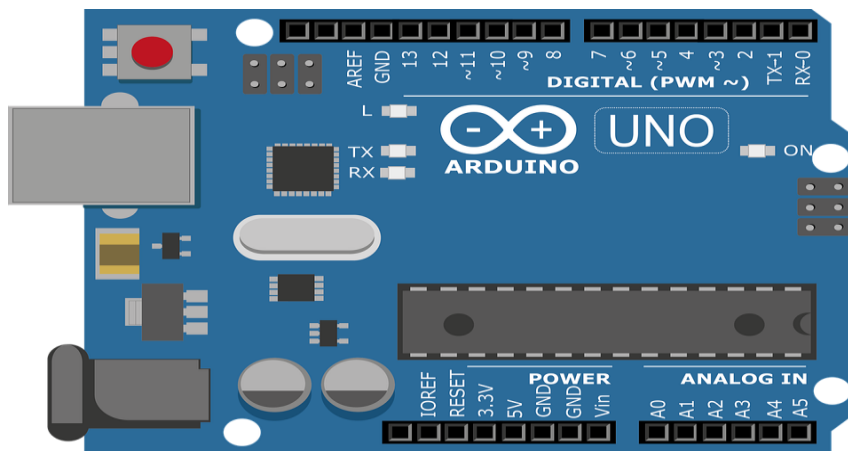
- USER INTERFACE
- WEB SERVER
- HARDWARE INTERFACE

USER INTERFACE

The Web browser is the User Interface via which the user communicates and gives signal to the devices. An HTML response is sent to the Arduino UNO as soon as the user sends any data over the Internet. The Web page provides a graphical way to monitor the devices and also control them. The user opens a URL on the Web browser from any Internet connected device and selects an operation for a particular home appliance and submits the response.

WEB SERVER

The data received from the user Interface or from the Sensors are processed by Arduino UNO micro- controller. The Arduino UNO is a programmable circuit board which has an extensive use in various fields. It is a self-contained board which can be interfaced with a computer/laptop via USB cables etc. It is used as a Web Server and is connected to a Wi-Fi router via Wi-Fi Shield. Using this shield, Arduino is linked with the internet and further provide various built-in libraries which helps in surfacing a web interface on a web browser. Now, the data from the Web page (User Interface) is sent to the router and the Arduino using port-forwarding and Wi- Fi Shield. Arduino is programmed with Embedded C to send corresponding IR signal to the device. This is the main platform using which the user gets the flexibility to monitor several home appliances. Arduino starts the connection whenever an attempt is made to reach the URL from the internet browser. The Wi-Fi Shield initiates the connection using Static IP address. And then after creating a virtual server enables it to run on dynamic address. But to reduce the cost by a significant amount use of ESP8266 serial port Wi-Fi module is used as the shield which has same functionality but with only main features available.

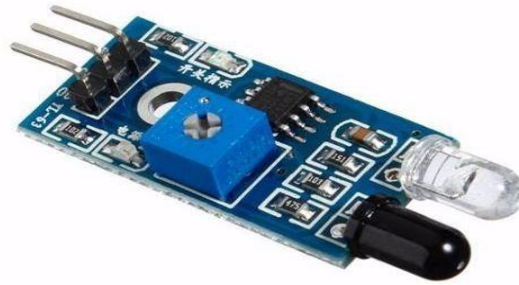


HARDWARE INTERFACE

This module consists of actuators and Sensors along with the electrical components to be automated for regulation.

IR SENSORS

With this IR receiver one can obtain the codes for different A/C models. It makes it possible to send IR signal to devices. This is attached to Arduino using add-on module. It can send different IR signals depending upon different operations.



Conclusion & Future scope

In the design proposed above we have implemented a Wireless home automation control system using Arduino Uno microcontroller which is very simple and feasible to use. For the web application various web technologies (HTML & CSS) is provided to provide simple reflexive UI. This makes work easier for users by complete automation of necessary various appliances and other components. The safety of user is considered and hence wiring the devices with server is done with utmost care. Further in this current system we can build cross platform system that can be deployed on android, iOS, Windows etc. Limitation to control only necessary devices can be removed by automating all other home appliances. Security feature can also be done by installing cameras, allowing the user to observe activity around a home as in [7]. System can also include motion sensors that will detect any kind of unauthorized, suspicious movement and notify the user immediately. Moreover appliances can be handled using spoken commands and hand gestures.

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AUTOMATIC PLANT IRRIGATION SYSTEM USING ARDUINO

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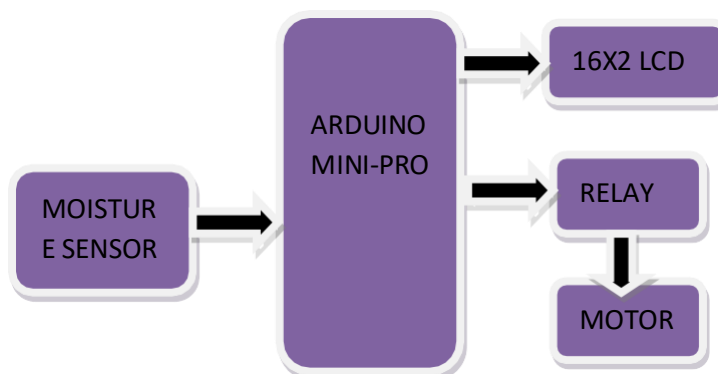
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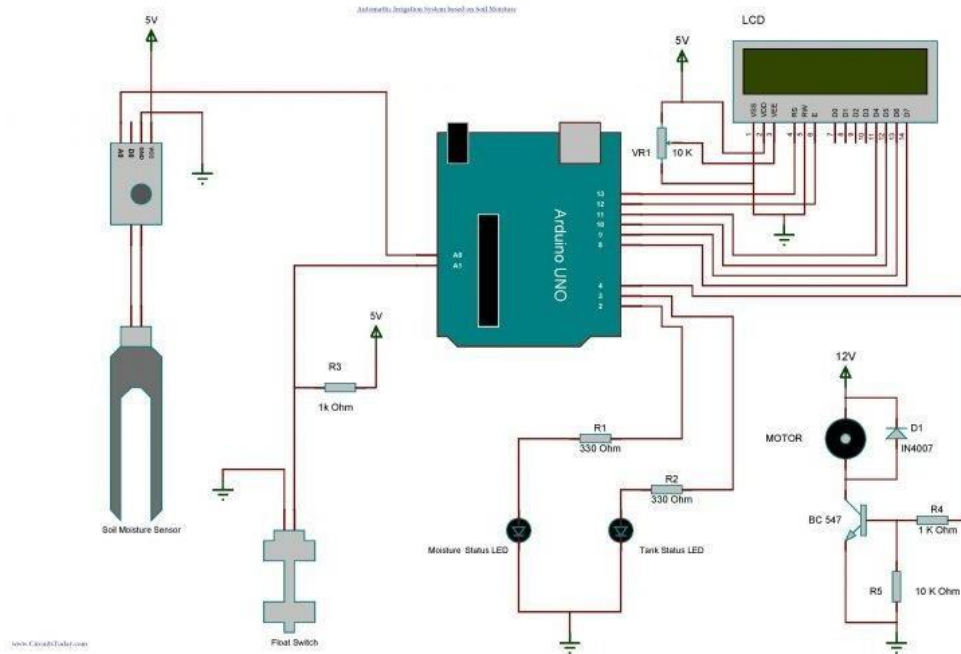
ABSTRACT:

Now a days its a challenge to improve development of plant in respect of its growth and to reduce costs which leads to an innovative idea of using an automated irrigation system which will further help in better management of water and human resources. An automated irrigation system have been developed using sensors technology with Arduino to efficiently utilize water for irrigation purpose. The system has soil moisture sensor inserted into the soil of the plants and a water level sensor placed in a water container from where water will be pumped to plants for irrigation. An algorithm has been build out with threshold values of soil moisture sensor to control the water quantity in soil and also a water level sensor has been implemented to measure the water level in tank. This project requires Arduino board having inbuilt ATmega328 microcontroller. This project is need of the hour to convert manual irrigation into an automated irrigation which with the help of soil moisture sensor will detect dankness content of soil leading to turn ON/OFF of pumping motor. Human efforts can be reduced using this technique and increase saving of water by efficiently irrigating the plants. The design has been made with better resource management and low power consumption. This project brings into play a micro-controller which is of 8051 family, this programmable micro-controller collects the input signals converted into values of moisture in the soil via soil moisture sensors. As the microcontroller starts obtaining the signals, it creates an output that forces a relay for running the water pumping motor. An LCD screen is also linked to the micro-controller to show moisture conditions of the soil and water pump. The water level sensor is used to detect the level of tank so that tank contains efficient water to transfer into crops.

BLOCK DIAGRAM:



CIRCUIT DIAGRAM:



NEED OF AUTOMATIC IRRIGATION

Automatic irrigation system proves to be very helpful for those who travel. If designed and coded properly, automatic irrigation systems can be very cost effective and can do a lot of water conservation. Watering with a pipe or with oscillator wastes water and none of these method aim plant roots. Automatic irrigation systems can be designed in such a way which gives required amount of water in a targeted area, and which will also promotes water conservation.

LITERATURE REVIEW

In this paper, soil moisture sensor is placed in the root zone of plant/field. The sensor sends information and transmits the data to the microcontroller. An algorithm was developed to measure threshold value soil moisture sensor that was programmed into a microcontroller to monitor the humidity content of the soil. This paper designs a model of automatic irrigation system which is based on microcontroller ATMEGA328. Temperature and soil moisture sensors are placed in the field. Sensors sense the moisture content of the soil and give the information to farmer through GSM Module. Farmer gets to know the status of the pump installed in the field via GSM Module without going into the field. When the moisture content reaches above the desired threshold value the pump automatically turns off and the message is conveyed to the farmer.

- Humidity/Soil Moisture Sensor: The humidity/soil moisture sensor just senses the humidity or the moisture of the soil. The change in humidity is proportional to the amount of current flowing through the soil.

- Diode (In4007): It allows unidirectional flow of current/power supply to the system.
- Potentiometer: It is used to control the contrast of the LCD display.
- Voltage Regulator Ic7805: Voltage regulator IC converts fluctuating ac voltage in to constant dc voltage.
- Temperature Sensor (Lm 35): LM35 sensor is used to record the atmospheric temperature which is then displayed on LCD.
- Microcontroller Atmega 328: It is a single chip microcontroller. This 8 bit microcontroller has 32kB flash memory with read-write features. It has 32 general purpose working registers, and 3 flexible timer counters .It also has internal-external interrupts and serial programmable USART.
- Oscillator: A 16MHz oscillator is used to provide constant non-fluctuating frequency to the microcontroller.
- Motor: Motor is used to indicate the on/off state of pump when soil is wet/dry. It is controlled by microcontroller as programmed.
- LCD (16x2): This is the first interfacing example for the Parallel Port. It is used to display the current statistic on the screen.
- Power Supply: Power supply of 12V is used for running this hardware system.
- Reference Voltage: It is the ideal defined voltage.

RESULTS AND DISCUSSIONS

The system used provides us with the readings of the temperature of the atmosphere along with the humidity content of the soil. These data are used to keep a track of the requirements if the field and to keep a check on the proper functioning of the system. Automatic plant irrigation system is basically designed for the introduction of the embedded technology in irrigation sector. This system will help the farmers to reduce their work pressure. This system will be helpful for the farmers to save their precious time and can yields more crops. Certainly it will be helpful for the farmers in improving their economical condition.

CONCLUSION

The automatic irrigation control using arduino uno has been experimentally proven to work satisfactorily and we could successfully set the timer and managed to control the motor over time.This process not only records values of temperature and humidity it also controls the motor accordingly.Analyzing the weather condition motor will automatically maintain water supply making it possible to maintain greenery without human intervention.

FUTURE WORK

Using this system as framework,the system can be expanded to include various other options which could include mobile application control of motor and wi fi controlled monitoring. These will expand the working capability and efficiency of this prototype.It can be implemented not in

agriculture but in gardens in any places using the sprinkler concept. It has a vast scope when it is mixed with IOT. Automation will get a new dimension through this.

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AIRPOLLUTION MONITORING SYSTEM USING ARDUINO

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ABSTRACT:

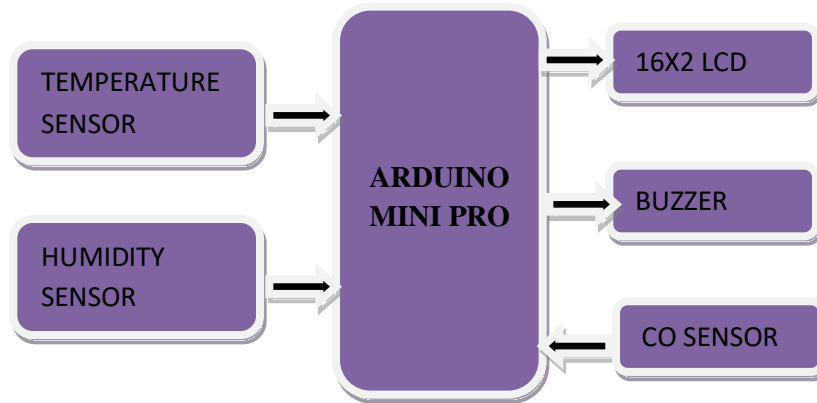
The level of pollution has increased with times by lot of factors like the increase in population, increased vehicle use, industrialization and urbanization which results in harmful effects on human wellbeing by directly affecting health of population exposed to it. In order to monitor In this project we are going to make an Air Pollution Monitoring System in which we will monitor the temperature, humidity and co that will trigger a alarm when the air quality goes down beyond a certain level, means when there are sufficient amount of harmful gases are present in the air like CO₂, smoke, alcohol, benzene and NH₃. It will show the air quality in PPM on the LCD

INTRODUCTION

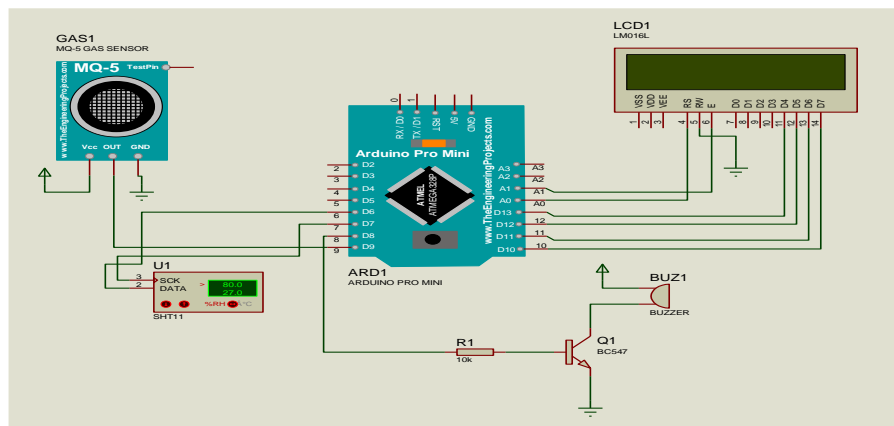
Air pollution is the presence of extra unwanted biological molecules, particulates or other harmful things into the earth atmosphere. It is a major cause of infections, allergies, and eventually reasons of death to some peoples.

It also harms to other existing creatures like that animals as well as food crops, or the ecological or built environment [1-2]. They are also accountable for various kinds respiratory infections (like asthma), causes of different types of cancer in individuals, if they are unprotected to these toxins or chemicals for long period of time. For example, carbon monoxide (CO) is extremely poisonous to people as it may happen serious asphyxiation, headaches because of the composition of carboxy-hemoglobin and thus a reason of death if unprotected for a long time. The world health organization (WHO) in 2014 approximated that 7 million people deaths worldwide because of air pollution. The similar approximation roughly equaled by the International Energy Agency (IEA) also [3]. These chemicals or pollutants are also responsible for various environmental calamities like acid rain and depletion of ozone layer. Because of a number of anthropogenic actions, air pollution is on the growth and its controlling is of significant importance to alleviate particular actions to limit it.

BLOCK DIAGRAM:

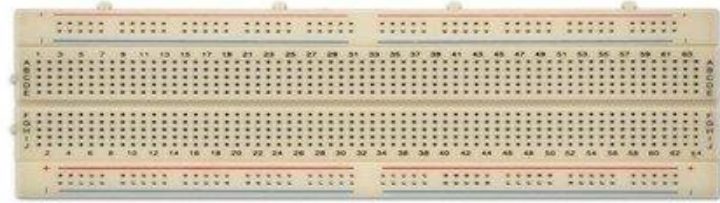
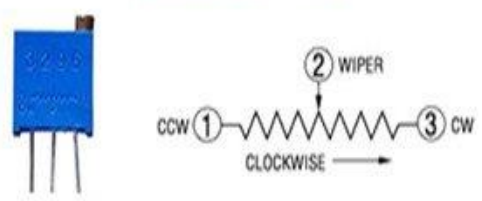
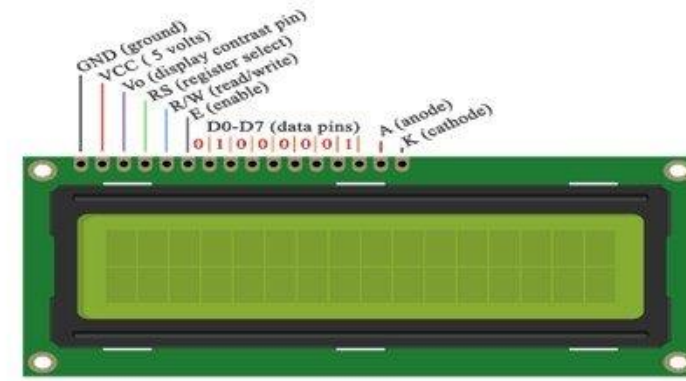
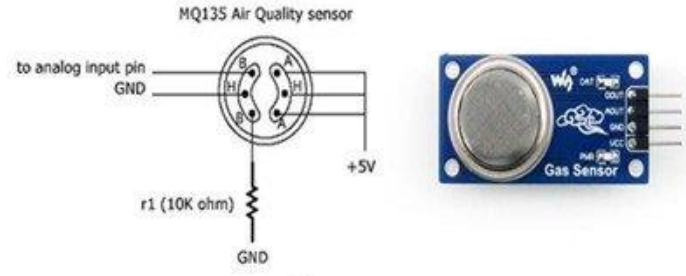
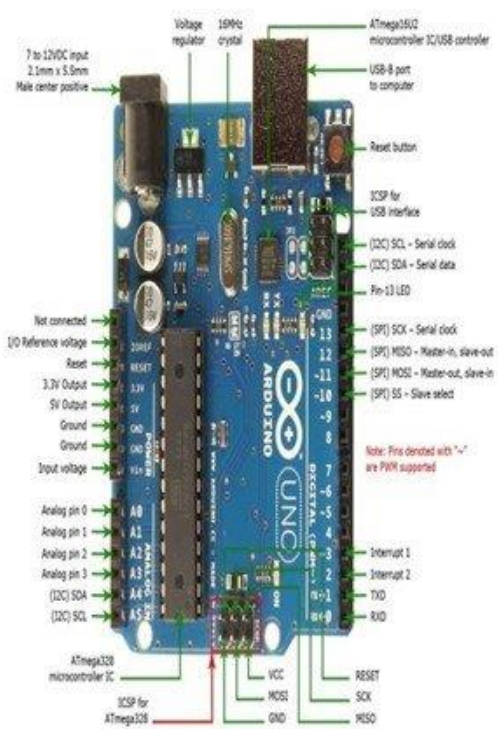
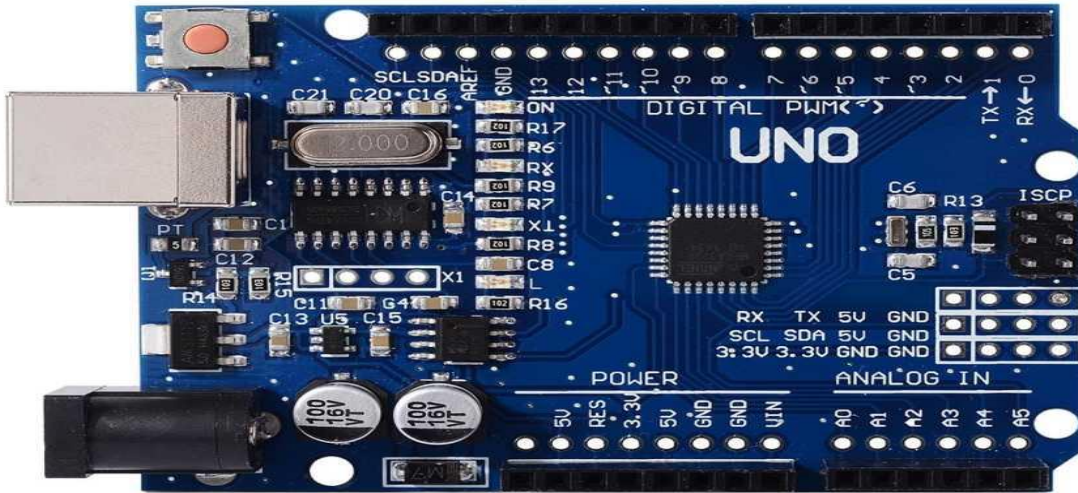


CIRCUIT DIAGRAM:



METHODOLOGY

We have used Arduino UNO, air quality sensor, LCD display, breadboard, jumper wires, and potentiometer to develop an arduino based air pollution detector which combined a small-sized, minimum-cost sensor to an arduino microcontroller unit (Figure 1). The device is linked to a computer through a serial connection. From the sensor, the collected data through the arduino microcontroller. It will then be transmitted to the computer software, where it becomes documented and plotted in real-time. It is very small in size and can be hand-held measurement system that can detect numerous gas in real time.



PARTS OF AIR QUALITY MONITOR SYSTEM

WORKING

The major chip of the system is LM393 and MQ135 are gas sensing analysis [8, 9, 10]. The Arduino or Genuino Uno is a modern microcontroller board based on the ATmega328P. It is simply related to a computer by a USB link or power. Connected to an AC-to-DC convertor or battery source to become commenced [10-11]. Using jumper wires the MQ135 gas sensor unit is linked to the Uno board. The sensors analog pin is then related to the analog pin 0 and digital pin to digital 8 on the arduino board, while +5V and the GND (ground) pins on the sensor unit are linked to the 5V Vcc and GND (ground) pin correspondingly on the arduino board. Using USB connection, the arduino Uno board is then linked to a computer system. This part elaborates the hardware and software instruments and structural design of the detector.

CONCLUSION

We have developed an Arduino based air pollution detector which is a very effective air pollution monitoring system. Based on the performance we can say that it is easy to use, and functionality is comparable to the expensive existing air pollution detectors. It is a microcontroller based portable system. It is efficient and user-friendly air quality detection system.

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Detector/